COMPARISON OF SPIN HALL EFFECT (SHE) AND SPIN TRANSFER TORQUE (STT) MAGNETIC RANDOM ACCESS MEMORIES (MRAMs)

F. LAARIEDH*, A. LTAIEF, T. B. BADECHE, A. H. LAATAR
Department of Physics, Faculty of science, University of Tabuk, Tabuk 71491, Kingdom of Saudi Arabia

High performance, non-volatility (NV) and high density are the three boons required for today's microelectronic systems. Magnetic Random Access Memory (MRAM) is a promising candidate to be the universal storage device. The Magnetic Tunnel Junction (MTJ) is the cornerstone of the NV-MRAM technology. The MTJ can be based on Spin Transfer Torque (STT) switching which is considered as a hot topic for academic and industrial researchers the last decade. Moreover, the Spin Hall Effect (SHE) based MTJ has recently been considered as an interesting device offering an increased reliability thanks to independent write and read paths. Since both MTJ devices (STT and SHE) seem to develop the data storage market, it is crucial to compare their capability when integrated with advanced CMOS processes in terms of transistor sizing and performance. Based on the state of the art, we supposed that it is possible to reach a mature magnetic processes that would enable to fabricate small junctions. Simulation results have been driven with 28 nm CMOS process. We showed that at that CMOS node, it is possible to furnish the required writing current with equitable size of transistors and so achieving high density MRAMs. At 28 nm node, the minimum transistor size can be used by the STT device. Although it is not the case for the SHE device, it achieves a remarkable gain in term of energy which is 5x better compared with the STT technology. Results are promising for high performance and high density hybrid magnetic/CMOS integrated circuits (ICs).

(Received May 17, 2017; Accepted August 8, 2017)

Keywords: Magnetic Random Access Memory, non-volatility, Magnetic Tunnel Junction, Spin Transfer Torque and Spin Hall Effect.

1. Introduction

An ideal storage device should combine the high density of Dynamic RAMs (DRAMs), the rapidity and robustness of Static RAMs (SRAMs) and the non-volatility (NV) of Flash memories. It seems that the intensive progress in spintronics domain refreshes the dream of IC designers to consider such a universal memory which gathers most merits encountered separately in existing random access memories (RAMs). Magnetic RAMs known as MRAMs are based on Magnetic Tunnel Junctions MTJs. They also offer high endurance and intrinsic hardness to radiation. Besides, the NV feature of MTJs makes them very attractive for Application Specific Integrated Circuits (ASICs). For instance, NV flip-flops can be designed to be used as a primitive cell into the ASIC design library offering safety, power reduction and instant on/off [1]. By view of this fact, both memory and logic design communities are interested in the integration of MTJs with CMOS circuits.

The switching mechanisms of MTJ determine the power, speed and area performances of hybrid MTJ/CMOS circuits. The early generation of MTJs commercialized by Everspin, was based on Field Induced Magnetic Switching (FIMS) [2] writing scheme. A later improvement was proposed by Crocus by thermally assisting the writing operation (TAS) [3]. The high switching current of FIMS (>10mA) and TAS (>1mA) limits significantly their future use for memory application and bring the dynamic power issue for the logic circuits. A great interest is now given

* Corresponding author: flaariedh@ut.edu.sa

for the Spin-Transfer Torque (STT) switching approach which requires a lower current (e.g. <100 µA) to reverse the state of MTJ [4] [5]. The high scalability of STT-MTJs opens up new horizons for commercial applications of hybrid MTJ/CMOS circuits. However, the 2-terminal structure of the STT device exhibits a common write and read path. This hints two major shortcoming limiting the reliability of the device; i) the high current density required for writing can occasionally damage the MTJ barrier, ii) it remains a challenge to fulfill a reliable reading without ever causing switching. Recently, in 2011, the possibility of a fourth magnetization switching approach known as "Spin Hall Effect" (SHE) has been proved [6]. Such a writing scheme uses an in-plane induced current to reverse the state of the MTJ without passing through the junction. The 3-terminal geometry of the SHE device separates the writing path from the reading path, thus the reliability issues encountered with the STT-MTJ are omitted.

Following the evolution of MTJ devices, current research is mainly focused on SHE and STT switching. It is expected that the potential of MTJ based circuits is enhanced at advanced nodes. In this work, we study the compatibility of MTJs with advanced CMOS processes and we compare their capability in term of performance and density using a 28 nm CMOS design kit. The SHE and STT technologies are compared in terms of the required MOS transistor size and the writing energy per bit cell.

Section 2 gives a brief description of both STT and SHE devices and explains the difference of their writing operation. In section 3, we evaluate the required transistor size per bit cell as well as the required energy to write the MTJ. Section 4 is the discussion.

2. Structure and writing mechanism of STT and SHE devices

The basic structure of an MTJ device is composed of 2 Ferro-Magnetic (FM) layers separated by an insulator (barrier). Both layers have an intrinsic magnetization. The first FM layer (hard layer) -with a pinned magnetization- acts as a reference while the second FM layer (soft layer) -with a free magnetization- acts as a storage layer, figure 1 (a). The magnetization of the storage layer can be switched between two stable states, either parallel (P) or antiparallel (AP) with respect to the reference layer. Electrons can tunnel through the thin barrier (~1nm) when a bias voltage is applied between the two electrodes of the device. The MTJ resistance is low (or high) for a P (or AP) magnetization configuration. Devices based on Perpendicular magnetic anisotropy (PMA) materials have an improved thermal stability and scale better than in-plane magnetic anisotropy (IMA) material-based [4] [5]. Thus, both STT and SHE MTJs studied in this letter are PMA materials-based.

Fig. 1 (b) shows the 2-terminal architecture of the STT-MTJ with the same read and write path. Figure 1(c) shows the SHE-MTJ with a 3-terminal architecture alleviating the stress on the barrier by separating the read path from the write path.

The switching mechanisms of STT and SHE devices have been widely discussed in literature and many macro models have been proposed to describe the behavior of such devices [4][5][7][8][9][10]. In this study, compact models have been used for each technology. Both STT and SHE compact models are developed according to the same magnetic assumptions in table 1.

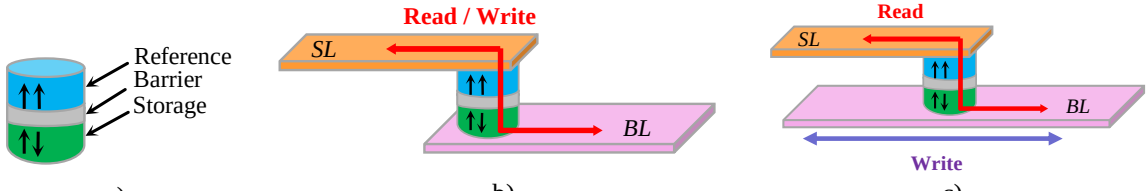

Fig. 1. Structure of the MTJ bit cell (a) Basic structure of the MTJ (b) 2-terminal STT device with common read and write path (c) 3-terminal SHE device with two independent paths for write and read operations. In-plane current injection through the write line induces the perpendicular switching of the storage layer

3. Evaluation results

A basic key toward MTJs perfection is the materials engineering development and magnetic processes optimization. Increasing the thermal stability, decreasing the switching current, maintaining a solid switching probability and keeping high reliability are the golden rules when scaling MTJ devices.

Many papers investigated sub-100 nm STT-MTJ samples and modeled their behavior to drive predictive studies at an extended scalability [5]. To the best of our knowledge, the smallest feature size of a STT-MTJ ever reported is 17 nm [11]. The sample was fabricating by using perpendicular materials with high interface anisotropy of 2.5 erg/cm² and improved integration processes. The fabricated device achieved reproducible switching with critical current (Ic) of 44 µA at 100 ns writing pulse, tunneling magneto-resistance (TMR) ratio of 70% and thermal stability factor (E/k_BT) of 34.

Concerning SHE-MTJs, the concept is much younger than its STT counterpart. At first, it has been reported in 2011 [6]. Since then, it has become a hot topic in both academics and industrials. Samples with a variety of materials combination have been fabricated [12][13][14][15] and physical models have been proposed to understand the behavior of SHE devices [7][8][9][10]. While the MTJ barrier material could be MgO or AlO_x, the writing electrode heavy materials existing in literature to fabricate the SHE device are: Tantalum (Ta), Tungsten (W) or Platinum (Pt). The spin hall (SH) angle and the resistivity are the two main material characteristics which matters for the SHE-MTJ; The SH angle determines the spin injection efficiency of the material. The resistivity of the material plays a fundamental role in the minimization of the writing energy since it determines the resistance of the writing path. The smallest dimension of the SHE device published in literature is a (135 nm × 135 nm) MTJ on top of a writing stripe of 210 nm of length, 135 nm of width and 3 nm of thickness [12]. In [13], it has been shown that the spin hall injection efficiency (ratio of spin current injected to the charge current in the electrode) as a function of electrode thickness has an optimum value at 2-3 nm electrode thickness. Concerning the current density to switch the magnetization, both theoretical models and experimental results agree on the fact that a magnitude of ~2×10^{12} A/m² is required for fast switching (≤ 1 ns) [7][8][9][10][11][12].

In our study, we target fast switching applications of NV-MRAM. Thus, the values of critical currents calculated in table 1 correspond to a switching operation of 1ns pulse.

This faithfully corresponds to the dimensions of MTJs we aim to evaluate. All assumptions about the parameters and the electrical performance shown in table 1 correspond closely to results published in literature about the SHE and STT devices. The minimum transistor width allowed by the used CMOS process is 80nm.

Table 1: Comparison SHE and STT bit cells to write with 1ns pulse and 1V power supply: required transistor size and writing energy per bit-cell

Devices parameters	MRAM technology	
	SHE	STT
Dimensions of the writing metal (length, width, thickness) (nm)	(46, 28, 3)	-
Resistivity of the writing metal µΩ.cm (Pt, Ta, W) [13]	(20, 190,	-
Saturation magnetization (A/m)	1.08×10^6	1.08×10^6
Damping factor, α [13]	0.6	0.01
Spin Hall angle (Pt, Ta, W), Θ_{SHE} [13]	(0.07, -	-
Parallel resistance Rp (KΩ) with RA @ (0V,300K) = 5.8 Ω.µm²	9	9
Jc (A/m^2)	2×10^{12}	7.2e10
Ic (µA)	150	50
MOS Transistor Width (nm)	180	80
Writing energy (fJ)	4	20

4. Discussion

The writing operation of MTJs, 1 MTJ is usually associated to a selection transistor to make 1 bit-cell architecture. At a given supply voltage (V_{dd}), the size and the polarization of the transistor determine the amount of current which flows through the junction. To keep the high density feature of MTJ-based MRAMs, it is not judicious to use a large bit-cell transistor for each MTJ. Table 1 shows that smaller transistors are required for the STT device at both nodes when compared to its SHE counterpart. This is mainly due to the high current density (and consequently the writing current) required to switch SHE-MTJs. At 28 nm dimension, STT-MTJ based circuits could be designed with the minimum transistor size (80 nm transistor width). Such a result opens the doors for ultra-dense MRAMs and eases the integration of STT-MTJ in full digital design flows. In general, results concerning the size of transistors required for both (STT and SHE) MTJs are still very reasonable at 28 nm scale, especially when compared with the 6 transistors required for the SRAM bit-cell. With the current state of art, the SHE device does not use the minimum transistor size. In one hand this decreases the bit-cell density, in the other hand the immunity to the CMOS process variation is enhanced since larger transistors are used.

As we explained in section 2, the writing mechanism of the SHE-MTJ is different from its STT counterpart since an in-plane current is applied through the stripe line conductor avoiding the passage through the junction. Thus, the electrical stress on the barrier is relaxed and endurance is improved. Benefits in terms of energy per bit-cell can be also observed; since, the writing stripe is highly conductive (Pt, W, Ta), the writing path has a very low resistance (R_w). If we consider Ic the critical writing current and τ =1ns the width of the writing pulse, the energy per bit-cell can be calculated as ($E= R_w \times Ic^2 \times \tau$). In our study, we consider the case of Platinum (Pt) with low resistivity value (20 $\mu\Omega$.cm). According to the geometry dimension ratios proposed in table 1, an improvement of 5× is observed in favor of the SHE device when compared with the energy required for the STT device. This ratio could be diminished if we use other heavy materials such as the Tantalum (Ta) or the Tungsten (W) which have a higher resistivity.

For a given applied voltage, the very low resistance of the write path offers the possibility to attain a high write current. When associated to the semi-processional switching nature of SHE devices [9][10], ultrafast speed can be attained. Experimental results of the SHE device show that it is possible to switch at only 380ps [12]. Theoretical predictive studies of the SHE technology proclaim that the SHE device can perform 4× faster with a decrease of 20× in term of energy [1] when compared with STT-MTJ. Also, a predictive study of an ellipsoidal SHE device with dimensions of (30 nm × 60 nm) claims that at low voltage, an improvement of more than 100× can be achieved in term of energy-delay [13].

Finally, it is worth noticing that in our study, we did not consider the process variation and devices mismatches. At very advanced nodes, both (CMOS and magnetic) processes suffer from a lack of maturity leading to a considerable process variations at the wafer level. Thus, the achievement of reliable and dense MRAMs is still related to the progress of materials engineering and the development of processes tools. At the design level, the proposal of robust MRAM architectures can alleviate some technological locks.

5. Conclusion

VLSI systems are suffering from high leakage current at advanced technology nodes. Using “hybrid CMOS/Magnetic" integrated circuits (ICs) could be a brilliant solution to overcome this problem. The integration of non-volatile memories, such as MRAMs, closer to the logic reduces the power consumption and increases the bandwidth between memory and logic. In this study, simulation results with MTJ dimensions of 28 nm for STT and SHE switching devices showed that the minimum size of transistor (80 nm width) can be used in the case of STT-MTJ based bit-cell with 28 nm technology node. The reasonable size of required transistors by bit-cell confirms the density criteria of MTJ based MRAMs at scaled dimensions. The SHE device overcomes its STT counterpart in term of writing energy by a factor of 5× but uses a wider transistors which leads to a decreased density. Depending on the application, the SHE based

MRAM is preferred for high speed circuits with lower energy dissipation, while the STT based MRAM offers a higher density.

Acknowledgment

The author would like to acknowledge University of Tabuk for the financial support under research project number S1437-127.

References

[1] K. Jabeur, Fabrice Bernard-Granger, G. Di Pendina, G. Prenat, IEEE electron device letters, **35**(3), march (2014)
[2] Everspin (2012). [Online] Available: http://www.everspin.com
[3] L. Prejbeanu, M. Kerekes, R. C. Sousa, H. Sibuet, O. Redon, B. Dieny, J. P. Nozieres, J. Phys, -Condens. Matter, p. 165218, (2007)
[4] W. Kang, W. Zhao, J-O. Klein, Z. Wang, Y. Zhang, Y. Zhang, D. Ravelosona, C. Chappert, 'An Overview of Spin-based Integrated Circuits, Proceedings of IEEE ASP-DAC, (2014)
[5] Ki Chul Chun, Hui Zhao, Jonathan D. Harms, Tae-Hyoung Kim, Jian-Ping Wang, Chris H. Kim, IEEE journal of solid-state circuits **48**(2), 598 (2013).
[6] I. M., Miron, K. Garello, G. Gaudin, P-J. Zermatten, M-V. Costache, S. Auffret, S. Bandiera, B. Rodmacq, A. Schhuhl, P. Gambardella, Nature **476**, 189 (2011).
[7] K. Jabeur, G. Prenat, G. Di Pendina, L. D. Buda Prejbeanu, I. L. Prejbeanu, B. Dieny, 'Compact model of a three-terminal MRAM device based on Spin Orbit Torque switching', ISCDG Proceedings, (2013)
[8] K. Jabeur, L. Buda-Prejbeanu, G. Prenat, G. Pendina, International Journal of Electrical, Electronic Science and Engineering, **7**(8), 497 (2013).
[9] Ki-Seung Lee, Seo-Won Lee, Byoung-Chul Min, Kyung-Jin Lee, 'Thermally activated switching of perpendicular magnet by spin-orbit spin torque', arXiv:1401.2266 [cond-mat.mtrl-sci], (2014)
[10] Ki-Seung Lee, Seo-Won Lee, Byoung-Chul Min and Kyung-Jin Lee, Appl. Phys. Lett. **102**, 112410 (2013).
[11] Woojin Kim, J. H. Jeong, Y. Kim, W. C. Lim, J. H. Kim, J. H. Park, H. J. Shin, Y. S. Park, K. S. Kim, S. H. Park, Y. J. Lee, K. W. Kim, H. J. Kwon, H. L. Park, H. S. Ahn, S. C. Oh, J. E. Lee, S. O. Park, S. Choi, H. K. Kang, C. Chung, 'Extended scalability of perpendicular STT-MRAM towards sub-20nm MTJ node ', pp (531-534), IEDM (2011).
[12] K. Garello, C. O. Avci, I. M. Miron, O. Boulle, S. Auffret, P. Gambardella, G. Gaudin,' Ultrafast magnetization switching by spin-orbit torques', arXiv:1310.5586v1 (2013)
[13] S. Manipatruni, D.E. Nikonov, I. A. Young, "Voltage and Energy-Delay Performance of Giant Spin Hall Effect Switching for Magnetic Memory and Logic", Cornell Univ. Press, pp1-16 (2013)
[14] L. Liu et al., Science **336**, 555 (2012).
[15] J. Guo et al, "MRAM Device Incorporating Single-Layer Switching via Rashba-Induced Spin Torque", IEEE transactions on magnetic **47**(10), 3868 (2011).