

CONDUCTION STUDIES ON EVAPORATED CADMIUM SULPHIDE THIN FILMS

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CdS thin films were prepared by thermal evaporation technique under vacuum onto glass substrates at different substrate temperatures with different gaps. The structure of the films was confirmed using X-ray diffraction (XRD). The deposited films were found to have a crystalline structure with hexagonal phase. The electrical properties were found to depend on the substrate temperatures. A significant increase of resistivity from 10^3 to $10^7 \Omega\text{m}$ and space-charge-limited current were observed in CdS films evaporated by vacuum evaporation. Ohmic behavior was detected at low voltage, on the other hand the space charge limited current (SCLC) was noticed at high voltage. The transition voltage (V_t) was varied with substrate temperatures and the distance of the gaps.

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1. Introduction

CdS is one of the most studied materials (II – VI compound) with a band gap of about 2.42 eV at room temperature [1, 2]. CdS is one of the important materials for application in electro-optic devices such as photoconducting cells, photosensors, transducers, laser materials, optical wave guides and non-linear integrated optical devices [3, 4]. CdS has proved to be an ideal material for use as the window layer of heterojunction solar cells with CuInSe₂ and CdTe due to its higher transmission and low resistivity [5, 6]. Also, it is widely used because it yields the transparent SnO₂ conducting electrode needed in the measurements. CdS can be doped with B, Al, Ga, and In to get n-type conductivity or with Cu, Ag, and Au to obtain p-type conductivity. But it is difficult to form p-type due to its shallow level. In addition, CdS is of n-type semiconductor with “intrinsically-disturbed stoichiometry”. It is well known that CdS thin films can exist in either cubic or hexagonal phase or as a mixture of both phases.

There are several preparation methods for CdS films such as sputtering [7], spray pyrolysis [8], thermal evaporation [9] and Pulsed laser deposition [10]. Among these, thermal evaporation under vacuum is one of the well established techniques. Some of the physical properties of vacuum evaporated CdS thin films are reported by various authors [11 – 13]. But little information on electrical properties of CdS film has been reported. CdS films prepared with thermal evaporation have an excellent photoconductivity as well as permeability in the visible range, but usually the resistivity is very high (over $10^8 \Omega\text{cm}$), which limits their use as optical window in solar cells. Annealing or chemical doping could solve this problem [14].

In the present study, CdS thin films are deposited by thermal evaporation under vacuum at different substrate temperatures and the films are characterized by X-ray diffraction (XRD) and electrical measurements. Hence the effect of substrate temperatures on the structural and DC electrical properties of vacuum evaporated CdS thin films is discussed.

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2. Experimental details

Thin films of cadmium sulphide (CdS) were deposited on glass substrates by usual thermal evaporation technique (Edwards E306A) at a vacuum pressure of 1.3×10^{-3} Pa (10^{-5} Torr). High purity (5N) bulk CdS powder (Fluka AG) was used for deposition of films at substrate temperature (T_s) in the range 100 – 200 °C. The film thickness (t) was measured by a mechanical stylus method (Sloan Dektak, model 11A). Gap type film geometry (Figure 1) with different effective gaps between the electrodes was made to facilitate DC electrical study. Pure indium (100 nm thickness) was taken for preparation of electrode films.

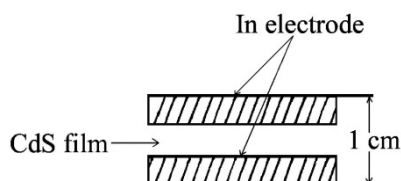


Fig. 1. Schematic diagram of cross section of the CdS structure.

X-ray diffraction (XRD) measurements were performed, using Ni filter and a monochromatic $\text{CuK}\alpha$ radiation ($\lambda = 1.5418 \text{ \AA}$) at 40 kV and 30 mA, with a slit of 0.2 mm, in a 60PA Jeol diffractometer. The scanning step was 0.01° with a counting time of 10 s. Data were sequentially collected in the range between 5 and 60° (2θ).

The electrical resistivity of the prepared films was measured by the four-point probe method of Van der Pauw with the required correction tables [15]. The current measurement was done by using high impedance Keithley 616 electrometer and auto-ranging stabilized power supply. The film was kept inside a continuously evacuated glass chamber during measurements.

3. Results and discussion

X-ray diffraction (XRD) was used to analyze the formation of the crystalline phases. XRD pattern of the as-deposited CdS thin films on glass substrates prepared by thermal evaporation are represented in Fig. 2 as a function of the substrate temperatures. From the pattern, it is clear that the films are polycrystalline in nature with a hexagonal structure of wurtzite phase. The XRD pattern of the as-deposited film shows the presence of a strong sharp peak at $2\theta = 26.44^\circ$. This could be indexed as (002) hexagonal structure. The XRD pattern of the film shows that the (002) peak height increases and peak width decreases as the substrate temperature (T_s) increases indicating an improvement in the crystallinity of the film. However, for the deposited film, an increase of hexagonal phase as T_s increased is evident from the appearance of other well defined hexagonal reflections.

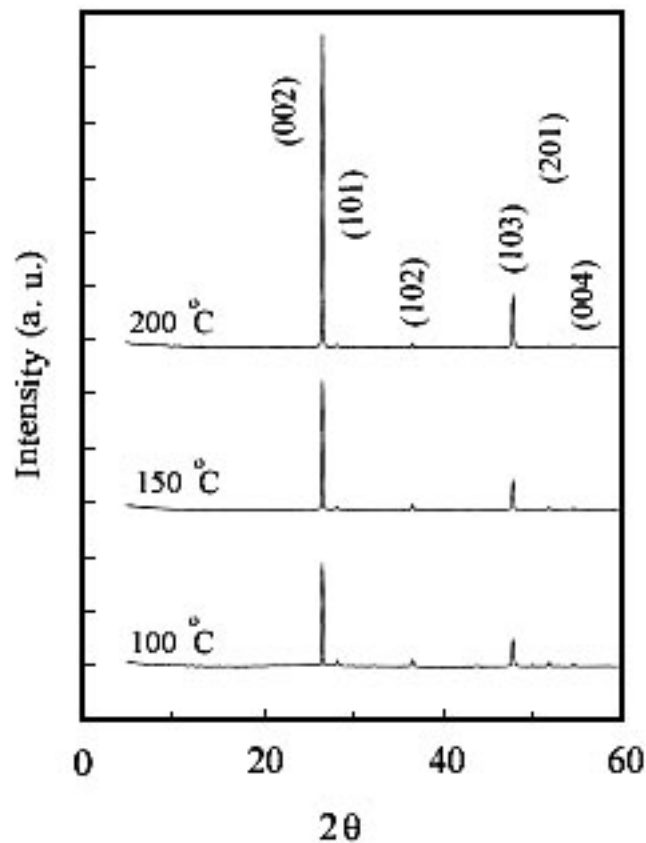


Fig. 2. XRD pattern of evaporated CdS thin film at different substrate temperatures ($t = 0.5 \mu\text{m}$, $R = 10 \text{ \AA/s}$).

The values of the lattice constants (a) and (c) were 0.4136 and 0.6713 nm, respectively. The (002) main peak always appears for all films. The other small peaks at different (2θ) which corresponds to the (101), (102), (103), (201) and (004) orientations, respectively, confirm the existence of the hexagonal lattice as reported elsewhere [16 – 18]. CdS films prepared by thermal evaporation technique always showed diffractograms with stronger intensity peaks, dependently of the substrate temperatures (T_s).

The average crystallite sizes of the grains (D) were determined from the (002) peak for all films using the Scherrer formula [19], assuming that microstrain can be neglected:

$$D = 0.94\lambda / \beta \cos\theta \quad (1)$$

where λ is the X-ray wavelength, β the full width at half maximum (FWHM) of the peak corrected for instrumental broadening, and θ the Bragg angle. The estimated average grain size of the as-deposited film with (002) plane is about 20 nm. Crystallite size measured in all CdS films is in good agreement to the reported values.

During measure of the electrical properties, a definite increase of resistivity (ρ) is noted from 10^3 to $10^7 \Omega\text{m}$ with substrate temperatures (T_s). This may be due to an increase of sulphur (S) partial pressure during evaporation. It is believed that this experiment is an evidence for the existence of sulphur vacancies in CdS thin films. This technique of thermal evaporation under vacuum is feasible and may be developed into a method for yielding CdS thin films of predictable resistivities. Further evidence of an improvement in the purity of CdS is the occurrence of space-charge-limited current in CdS thin films made by thermal evaporation technique.

Room temperature current – voltage (I – V) characteristics of the CdS structure is shown in Fig. 3 for different samples of varying substrate temperatures (T_s) ranging from 100, 150 and

200 °C. Indium [20, 21] ohmic contacts were made to this film by thermal evaporation under vacuum. Two distinct regions with different slopes are observed: at lower voltages up to the transition voltage (V_t) the slope of the log J versus log V plot was approximately equal to 1, while at higher voltage level, above a well-defined transition voltage (V_t), the slope was approximately 2. These slopes are typical of ohmic conduction at voltage below V_t and space-charge-limited conduction (SCLC) [22] at voltages above V_t indicates strongly the existence of traps by injected carriers.

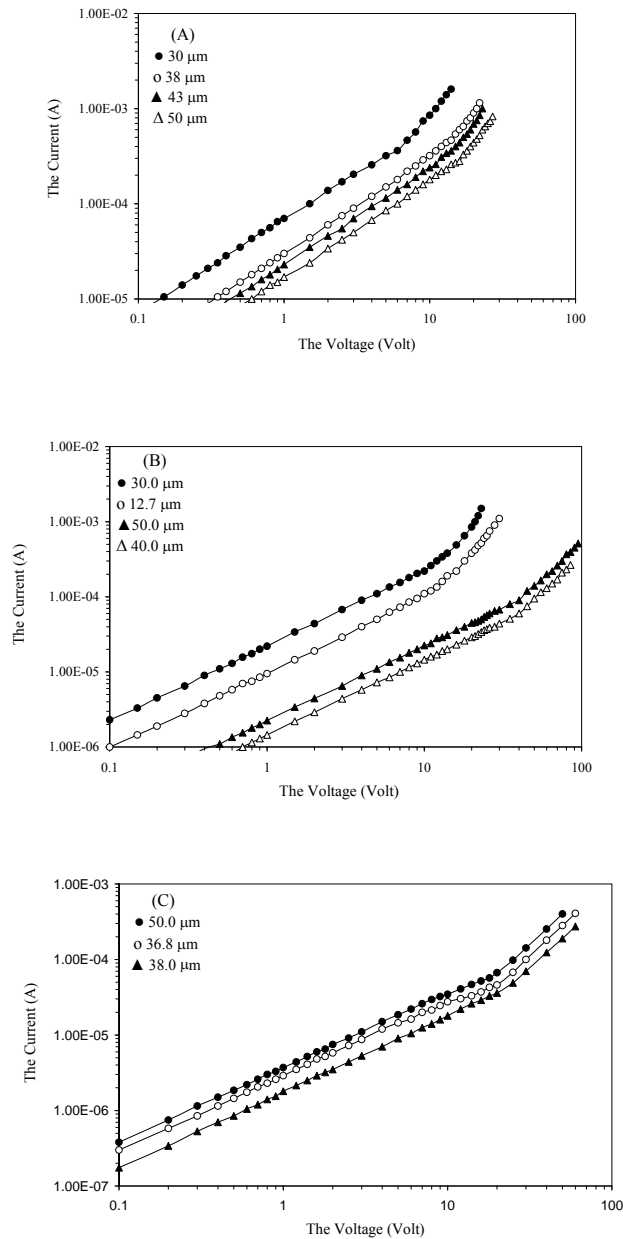


Fig. 3. The current-voltage characteristics of CdS at different substrate temperatures ($t = 0.5 \mu\text{m}$, $R = 10 \text{ \AA/s}$). A) $T_S = 100^\circ\text{C}$, B) $T_S = 150^\circ\text{C}$, C) $T_S = 200^\circ\text{C}$

If the ohmic conductivity is assumed at low – voltage region of ohm's law to be due entirely to electrons, the expression for the characteristic is [23]:

$$J = n_0 q \mu (V / L) \quad (2)$$

Where J is the current density, V is the applied voltage, n_0 the concentration of thermally activated electrons in the conduction band, q the electronic charges, μ the electron mobility and L the distance between the electrodes of the CdS.

Following the theory of Lampert [24], equation (2) is valid for the injection of one type of carrier only in the presence of a single – discrete trapping level. However, other trapping states may be present, but their density is such that they are incapable of dominating the statistics [25].

In order to estimate the value of n_0 , which may be readily determined from the slopes of the linear relations between J and V shown in Fig. 4, it is necessary to assume a value of $\mu = 18 \text{ cm}^2 / \text{V} \cdot \text{sec}$ [26]. Values of n_0 were found from 1.5×10^{11} to $7.5 \times 10^{12} \text{ m}^{-3}$ for the CdS films at different substrate temperatures. Thus, the values of n_0 at room temperature were found to influence with substrate temperatures, then also with the variation of the crystallite size. This is consistent with the conclusions reached by workers who have studied the electrical properties of CdTe [27] and CdS [28] samples. However, the influence in n_0 seems to be due to the variation in lattice imperfections and due to the increase of the grain boundaries. The values of n_0 are of two orders of magnitude lower than that of the previously recorded values of $(1 \times 10^{13} - 1.19 \times 10^{14} \text{ m}^{-3})$ for CdS films prepared by thermal evaporation [28]. It is possible to conclude that the lower values of n_0 determined in this work may be correlated with the crystallite size [29], and are also related to differences in impurity concentrations and energy levels resulting from the different preparation conditions [30].

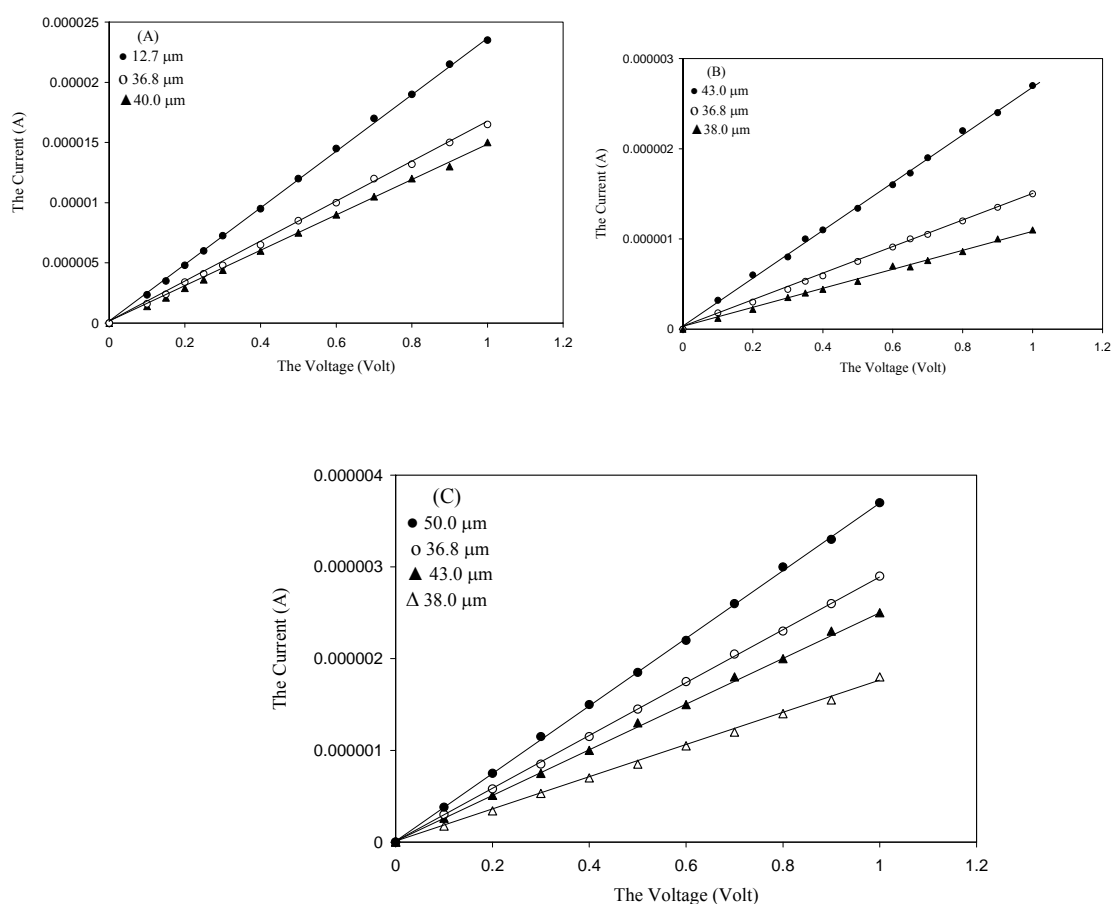


Fig. 4. Current – voltage relations at different substrate temperatures in the ohmic region ($t = 0.5 \mu\text{m}$, $R = 10 \text{ \AA/s}$). A) $T_S = 100^\circ\text{C}$, B) $T_S = 150^\circ\text{C}$, C) $T_S = 200^\circ\text{C}$

In the region of the higher voltage levels, the current is proportional to V^2 , indicating that the current is limited by space charge of carriers (SCLC) injected from the electrodes and is dominated by a single set of traps.

The current density, J , within the SCLC region and presented in Figure 3, is given by [31]:

$$J_{SCL} = (9/8) \epsilon \mu \theta (V^2/L^3) \quad (3)$$

where ϵ is the permittivity, μ the mobility, V the applied voltage and L the distance between the electrodes. θ is the ratio of free to trapped charge.

The values of θ may be estimated by plotting the relation J and V^2 as shown in Fig. 5. The calculated values of θ were found of $(2.5 \times 10^{-7} - 9.2 \times 10^{-9})$ with different substrate temperatures. This suggests an increase in trap concentration N_t . The increase of N_t cannot be interpreted in terms of the change of the crystallite size. This is because the size increases and consequently the grain boundary decrease as N_t increases. Therefore, the structural parameter which can be correlated with N_t is the preferred orientation. This is because the electric properties are measured in the (002) plane, which is the one of the highest atomic density in the wurtzite hexagonal structure of CdS. Then, the increase of N_t is due to the increase of the $\langle 002 \rangle$ crystallographic texture as proved by the structural study. Space charge limited conduction (SCLC) has been observed by different workers [32 – 35].

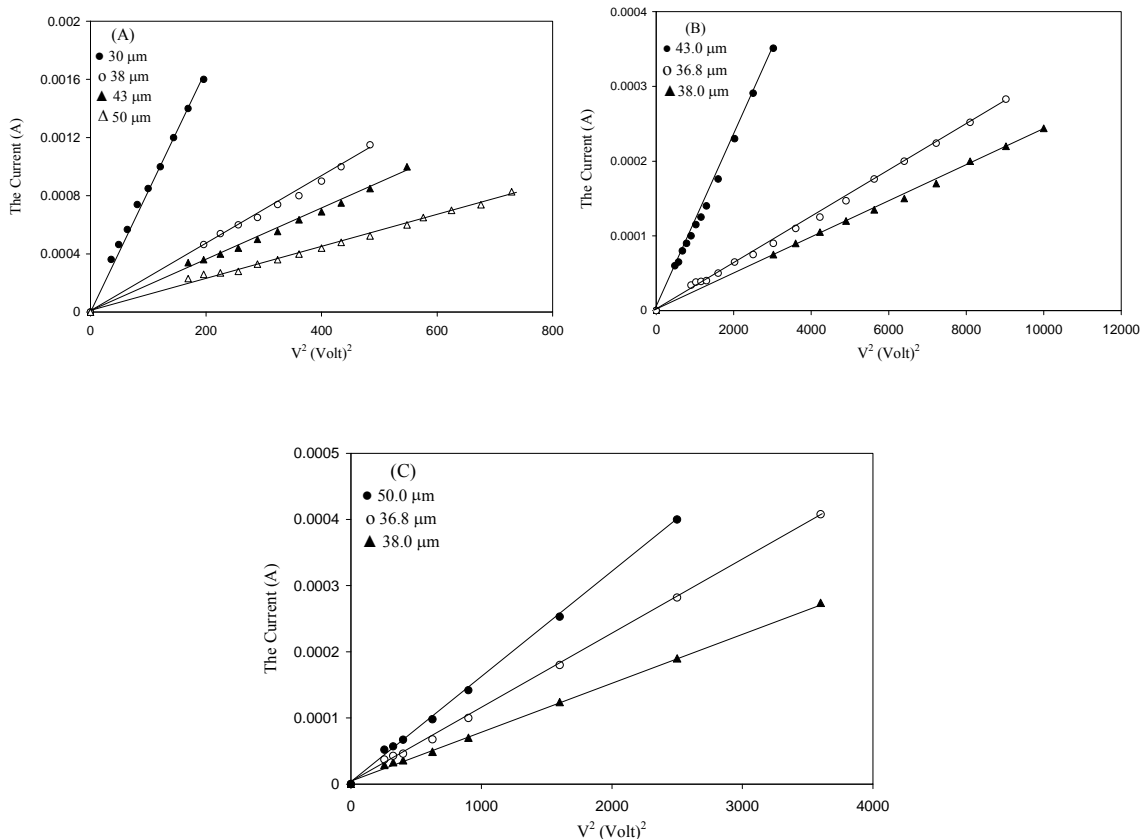


Fig.5. Current – V^2 relations at different substrate temperatures in the SCLC region ($t = 0.5 \mu\text{m}$, $R = 10 \text{ \AA/s}$). A) $T_s = 100^\circ\text{C}$, B) $T_s = 150^\circ\text{C}$, C) $T_s = 200^\circ\text{C}$

The transition voltage (V_t) at which the current converts from ohmic to SCLC behaviour, can be defined by equating the two currents in Equations (2) and (3) as

$$V_t = (8/9) (q / \epsilon) L^2 (n_0/\theta) \quad (4)$$

Evidently, V_t is expected to be proportional to L^2 and according the dependence of V_t on L^2 , shown in Figure 6, for substrate temperatures (T_s) ranging from 100 to 200 °C yields a straight line as predicted by equation (4). The estimated value of the slope ($8.0 \times 10^9 - 1.42 \times 10^{10} \text{ Vm}^{-2}$) was found to be nearly close to the calculated one $9.5 \times 10^{10} \text{ Vm}^{-2}$ using values of the derived parameters of n_0 , θ and ϵ quoted above.

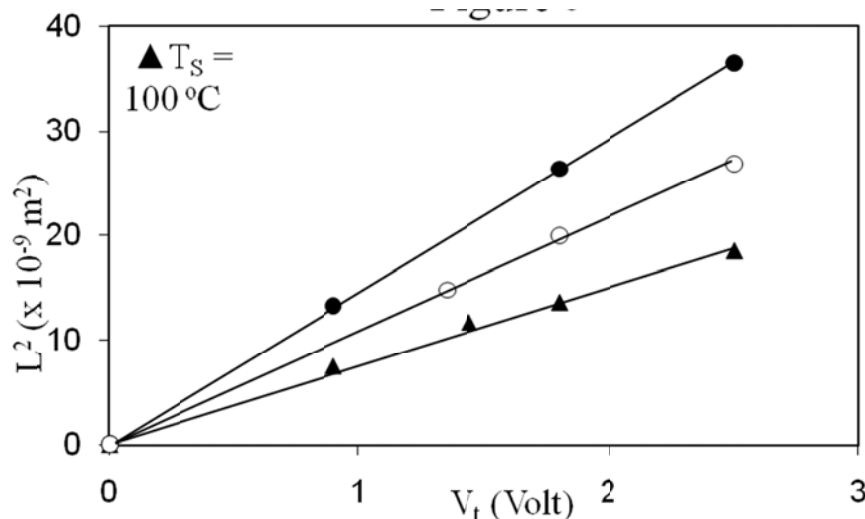


Fig. 6. Linear dependence of V_t on L^2 at different substrate temperatures, indicating the SCL conductivity ($t = 0.5 \mu\text{m}$, $R = 10 \text{ \AA/s}$).

On the other hand, the following equation, was used by Pizzarello [26] to estimate the number of traps (N_t):

$$V_t = q N_t L^2 / \epsilon \quad (5)$$

where N_t is the number of traps, L the distance between electrodes, ϵ the dielectric constant, and q the electronic charge. Calculating N_t from the value of V_t given in Figure 6 yields a value of $(4.9 - 8.9) \times 10^{18} \text{ traps/m}^3$.

The large difference between single – crystalline and thin films in the physical properties clearly is connected with the intergranular (grain boundary) scattering of the carriers in the CdS thin films. On the other hand, it should be noted that $I - V$ measurements taken in air on CdS thin films made by the thermal evaporation method do not show space-charge-limited current (SCLC), whereas measurements on the same sample in vacuum yield SCLC. The effect is probably due to gases absorbed on the surface that act as a shunt.

4. Conclusions

CdS thin films have been prepared by thermal evaporation under vacuum onto glass substrates at various substrate temperatures. X-ray studies of CdS thin films prepared by vacuum evaporation technique shows a (002) fibre texture and a crystallite size in the range of 20 nm.

Measurements of the electrical resistivity have indicated that the electrical resistivity in the range from 10^3 to $10^7 \Omega\text{m}$. Current – voltage characteristics have revealed that conductivity is ohmic at lower voltages and SCL conduction at higher voltages. Furthermore, results obtained within the SCLC region suggested the existence of a trap distribution dominated by a single-discrete trapping level. The transition voltage, V_t , between the ohmic and SCL conduction was

proportional to L^2 . Influence of n_0 seems to be due to the variation in lattice imperfections and due to the increase of the grain boundaries. However, the increase in the trap concentration, N_t , is expected to be correlated with increasing the degree of preferred orientation of the highest atomic density plane.

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