

## A SIMULATION MODEL APPROACH TO ANALYSIS OF HIGH BREAKDOWN VOLTAGE IN NORMALLY-OFF 4H-SiC VERTICAL JUNCTION FIELD EFFECT TRANSISTOR

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In this paper, the temperature dependent breakdown voltage characteristics of normally-off 4H-SiC VJFET (Vertical Junction Field Effect Transistor) are simulated using commercially based Sentaurus TCAD simulator. Newly developed impact ionization model is implemented to investigate the breakdown voltage. This physical based model proved to provide compatibility over the wide range of temperatures. The breakdown voltage indeed varies with temperature and device exhibits negative temperature coefficient. At gate doping of  $N_{\text{gate}} = 5 \times 10^{17} \text{ cm}^{-3}$ , the breakdown voltage of 14 kV is obtained with leakage current of  $2.1 \times 10^{-7} \text{ A}$ . Moreover, the simulation results indicate that with a gate doping of  $N_{\text{gate}} = 1 \times 10^{18} \text{ cm}^{-3}$ , the breakdown voltage of SiC VJFET is enhanced to 19 kV with leakage current of  $3.4 \times 10^{-8} \text{ A}$ . Using finite element simulation, the distribution of electric field and electron velocity as a function of temperature is also analyzed, which is not readily accessible by experimental techniques. The distribution of electric field revealed the punch-through behavior reported first time in our simulation case. In addition, 19 kV SiC VJFET showed 27% higher electric field when compared with 14 kV. The structure layout along with model validation showed that the breakdown voltage of 14 kV has an excellent agreement with experimental reported values.

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### 1. Introduction

For the advancement in power electronics towards faster and cheaper devices, semiconductor industries are moving towards high voltage, high temperature and high switching applications [1-2]. SiC has received attention because of its high breakdown critical electric field, high thermal conductivity and high saturation velocity. This can offer an alternative way to overcome the many obstacles. The high critical field of 4H-SiC leads to an increase in the breakdown voltage and is also responsible for the reduction of power loss [1, 3-5]. On the basis of this exceptional property, unipolar devices can provide excellent performance. SiC JFET is a good candidate because of no reliability issues unlike the gate oxide problems in SiC MOSFET [6-7]. Due to its industrial importance and use in commercial applications by different organizations, SiC JFET has become focused for future power electronics applications such as photovoltaic inverter, gate drive and hybrid electric vehicles which can operate at medium to high voltage [8]. SiC JFET has been investigated by various researchers to optimize the high breakdown voltage [9]. The high critical field of SiC is more efficient, which provides a thinner device, resulting in lower on-

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resistance [10]. Substantially, little work on modeling and simulations of SiC VJFET has been presented at high temperature [11]. Ref. [12] presented  $120\ \mu\text{m}/4.9 \times 10^{14}\ \text{cm}^{-3}$  drift layer doped design by experimental technique. The device has a capability to block 10 to 11 kV. They also presented a simulation and argued that the theoretical breakdown voltage which is 67.7% of experimental work. Ref. [13] and Ref. [14] experimentally studied the  $115\ \mu\text{m}/5.6 \times 10^{14}\ \text{cm}^{-3}$  and  $120\ \mu\text{m}/4.9 \times 10^{14}\ \text{cm}^{-3}$  drift layer doped designs in order to measure the high breakdown voltages of 14 and 10 kV, respectively. Ref. [15] designed  $100\ \mu\text{m}/8 \times 10^{14}\ \text{cm}^{-3}$  normally-on 4H-SiC VJFET and found efficient power switching device with high blocking voltage of 9 kV. In previous literature, high temperature effect is not studied and there were no descriptions about the finite element simulation, like 2D electric field and electron velocity distribution. Herein, we offer the  $120\ \mu\text{m}/6.0 \times 10^{14}\ \text{cm}^{-3}$  drift doping normally-off 4H-SiC VJFET which provided successfully high breakdown voltages of 14 and 19 kV, respectively. The other important parameters like electric field and electron velocity that relatively effective on the breakdown analysis, are also presented through finite element simulation.

## 2. Device structure

Fig. 1 shows  $120\ \mu\text{m}/6.0 \times 10^{14}\ \text{cm}^{-3}$  drift doped cross-sectional view of normally-off 4H-SiC VJFET. This device has spacing between two gates (channel width) embedded in the epilayer region, source and drain regions, and  $\text{SiO}_2$  as a passivation to protect the surface properties [16]. The importance of this design structure is moving towards toward the realization of high breakdown voltage capability which is strongly based on the design layout. It has been investigated that the design layout for breakdown characteristics is based on drift layer thickness and drift doping [17]. The other important parameters that also affect the device characteristics are the channel width and channel concentration. The design structure is created by the Sentaurus TCAD program [18]. This is commercial based software that particularly provides wide range of analysis such as transient response, device I-V characteristics, and internal visualization of device. For normally-off behavior, the vertical channel should be fully depleted in order to provide the desired breakdown voltage. The width and length of channel with concentration were selected to be  $1.25/3.5\ \mu\text{m}$  and  $5.0 \times 10^{15}/\text{cm}^3$ , respectively. It should also be emphasized that the gate doping concentration is also a critical parameter which define the normally-off behavior. Therefore, the boron doping concentration of  $1 \times 10^{18}\ \text{cm}^{-3}$  with vertical depth of  $0.6\ \mu\text{m}$  is selected for this simulation.

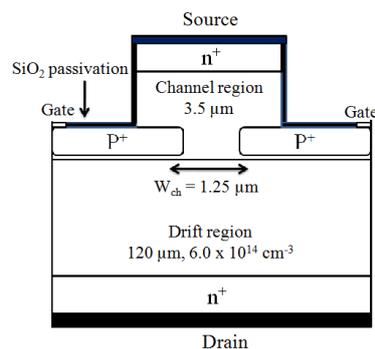


Fig. 1. Cross-sectional View of wider drift layer normally-off 4H-SiC Vertical Junction Field Effect Transistor.

## 3. Model approach

The Sentaurus TCAD is used to simulate the characteristics of 4H-SiC by solving the carrier continuity equation and poisson's equations as follows [19-20]:

$$\varepsilon \nabla^2 \psi = -q(p - n + N_D^+ - N_A^-) - \rho_1 \quad (1)$$

$$\nabla \cdot J_n = qR_n + q \frac{\partial n}{\partial t} \quad (2)$$

$$\nabla \cdot J_p = qR_p + q \frac{\partial p}{\partial t} \quad (3)$$

$$J_n = -q\mu_n n \nabla \phi_n \quad (4)$$

$$J_p = -q\mu_p p \nabla \phi_p \quad (5)$$

where  $R_n$  and  $R_p$  represent the recombination rate and  $J_n$  and  $J_p$  represent the electron and hole current density,  $\rho_1$  is the fixed charge density. In this simulation, the models for normally-off 4H-SiC VJFET selected from previous publications, included energy bandgap model, low field doping dependent mobility model, high field saturation mobility model, and incomplete ionization model. The new impact ionization model for the breakdown voltage simulation is implemented. Previously, different authors proposed different models to study the breakdown voltage analysis. The most important impact ionization models have been used, such as Okuto-Crowell model for 4H-SiC ultraviolet photodetectors [21] and Hatakeyama for the 4H-SiC Schottky diode [22]. But to the best of our knowledge, the Lakner model is used for the first time for the simulation of 4H-SiC VJFET.

The rate of generation for electron-hole due to presence of impact ionization is defined by

$$G^{ii} = \alpha_n n v_n + \alpha_p p v_p \quad (6)$$

where, and  $\alpha_n$  and  $\alpha_p$  represent the electron hole ionization rate. The Lackner model [18] used for the simulation is given by the following equations:

$$\alpha_{n,p}(F_{ava}) = \frac{\gamma a_{n,p}}{z} \exp\left(-\frac{\gamma b_{n,p}}{F_{ava}}\right) \quad (7)$$

$$z = 1 + \frac{\gamma b_n}{F_{ava}} \exp\left(-\frac{\gamma b_n}{F_{ava}}\right) + \frac{\gamma b_p}{F_{ava}} \exp\left(-\frac{\gamma b_p}{F_{ava}}\right) \quad (8)$$

$$\gamma = \frac{\tanh\left(\frac{\hbar\omega_{op}}{2KT_0}\right)}{\tanh\left(\frac{\hbar\omega_{op}}{2KT}\right)} \quad (9)$$

where,  $\hbar\omega_{op}$  represents the optical phonon energy and  $F_{ava}$  is the magnitude of electric field. Ref. [23] reported that  $a_n$  and  $a_p$  are the multiplicative coefficients, they vary linearly with temperature [24] are equal to  $1.98 \times 10^6 \text{ cm}^{-1}$  and  $4.38 \times 10^6 \text{ cm}^{-1}$ , respectively. While  $b_n$  and  $b_p$  are the critical field for both electrons and holes are equal to  $9.46 \times 10^6 \text{ Vcm}^{-1}$  and  $1.14 \times 10^7 \text{ Vcm}^{-1}$ , respectively.  $\gamma$  is a constant value is equal to 1.

#### 4. Simulation results and discussion

Fig. 2 shows the temperature dependent breakdown voltage characteristics in the temperature range from 27 to 500 °C. It has been investigated that wider channel opening required high negative bias for complete depletion in order to obtain high breakdown voltage. For this purpose, the negative bias of -6 V was used, which is limited to provide the optimum breakdown voltage of 14 and 19 kV as shown in Fig. 2(a) and 2(b), respectively. At  $V_G \leq -6 \text{ V}$ , no such significant variation in breakdown voltage was observed. In each temperature case, the breakdown

occurs when the ionization integral between the drain and source is equal to unity [25]. Note that the breakdown voltage decreases significantly with increasing temperature. This means that the device exhibits negative temperature coefficient for breakdown voltage [11]. It is quite obvious that low drift doping and high drift layer thickness restrict the breakdown characteristics at high temperature. In both cases, at 500 °C, the breakdown voltage is limited to 10.6 kV and 14.8 kV for 14 and 19 kV proposed design, respectively. It is important to note that for higher value of drift layer thickness, 14 kV SiC VJFET has good agreement with the experimental as well as theoretical data as shown in Table.

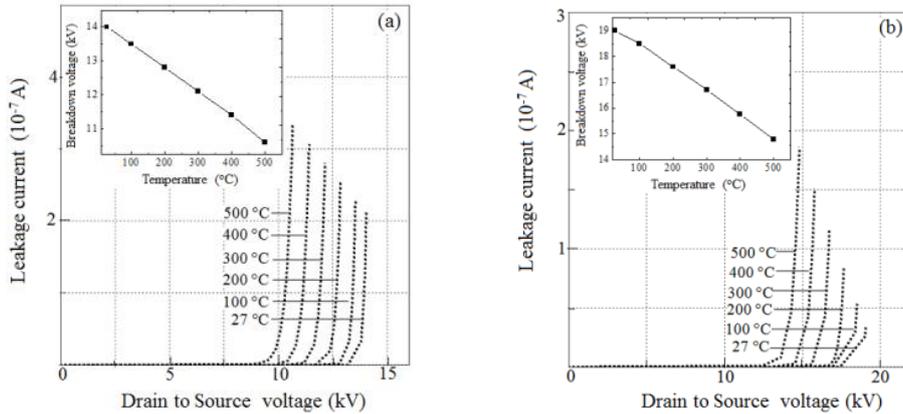


Fig. 2. Temperature dependence breakdown voltage characteristics at gate bias of -6V for (a) 14 kV and (b) 19 kV 4H-SiC VJFET.

Table 1 Comparative breakdown voltage with previous reported values.

References	Drift layer ( $\mu\text{m}$ )	Breakdown voltage (kV)
[12]	120	11
[13]	115	14
[14]	120	10, 15.7
[15]	100	9
Present simulation	120	14 and 19

The measured breakdown voltage of the proposed design as a function of drift doping concentration is shown in Fig. 3. The results indicate that the voltage driving capability is very high when drift doping is very low [17]. The breakdown voltage is almost the same under low drift doping for 27 and 500 °C as shown in Fig. 3 (b). Simulation results reveal that breakdown voltage decreases with the increase in drift doping. The high drift doping quickly reduces the dynamic space charge region which consequently to reduce the breakdown voltage. In both cases, breakdown voltage has no significance when doping concentration approaches  $10^{16} \text{ cm}^{-3}$ .

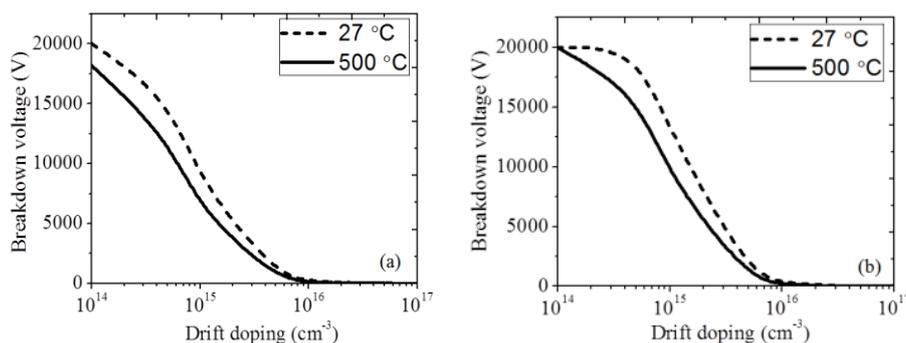


Fig. 3. Effect of drift doping on breakdown voltage at 27 and 500 °C for (a) 14 kV and (b) 19 kV 4H-SiC VJFET.

It is known that the breakdown voltage is significantly related to the critical electric field. The higher the electric field, maximum the breakdown voltage can be obtained [26]. We have simulated the vertical depth dependent electric field distribution at 27 and 500 °C for 14 and 19 kV VJFET. Since the surface is covered by the passivation of SiO<sub>2</sub>, and the doping level in the channel is one order of magnitude higher than that of drift region. Therefore, electric field is close to zero at the surface. We consider three layer structure p<sup>+</sup>-n<sup>-</sup>-n<sup>+</sup> in which p<sup>+</sup>-n<sup>-</sup> shows the gate-drift junction and n<sup>-</sup>-n<sup>+</sup> shows the drift-drain junction. The sharp overshoot in electric field was observed at the edge of gate as shown in Fig. 4. This effect is due to longitudinal electric field governed by p<sup>+</sup>-n<sup>-</sup> junction. The field approaches to maximum value of 2.8 and 2.2 MV/cm for 19 and 14 kV design, respectively as shown in Fig. 4 (a) and Fig. 4(b). A slight reduction in electric field was observed with increasing the depth of device provided nonzero electric field at n<sup>-</sup>-n<sup>+</sup> junction [27]. In an ideal case, the shape of electric field distribution should be triangular. If dynamic space charge region exceeds the drift depth the behavior is similar like trapezoidal. This effect is known as punch-through. The extant literature does not cover the issues related to punch-through in SiC VJFET. Concerning to other devices, the optimization of punch-through has been investigated. Ref. [28] experimented punch-through and non-punch-through behavior in the P-i-N power diode. They obtained the optimization of technological parameters related to the punch-through design. Ref. [29] found that the dynamic punch-through behavior is governed by the extension of the dynamically enlarged space charge region in the drift layer. They also found that the punch-through design is not suitable for high voltage application, because at this condition the device may be destroyed. Ref. [30] optimized the solution of breakdown voltage in 6H-SiC parallel junction. They optimized the punch-through in bipolar and unipolar devices. They also optimized the based width and doping in order to provide good validation related to punch-through design. By considering both junctions, the punch-through voltage can be expressed in the form:

$$V_{PT} = \frac{(E_C + E_1)t_{drift}}{2} \quad (10)$$

where, E<sub>C</sub> and E<sub>1</sub> represent the electric field at P<sup>+</sup>-n<sup>-</sup> and n<sup>-</sup>-n<sup>+</sup> junction, respectively. For 14 kV SiC VJFET, at 27 °C, the value of E<sub>1</sub> is found 0.52 MV/cm which decreased to 0.25 MV/cm at 500 °C. Similarly, for 19 kV, at 27 °C, the value of E<sub>1</sub> is found to be 0.95 MV/cm which decreased to 0.51 MV/cm at 500 °C. By addition of E<sub>C</sub> and E<sub>1</sub>, 27% of higher field for 19 kV was observed when compared with the 14 kV of breakdown voltage.

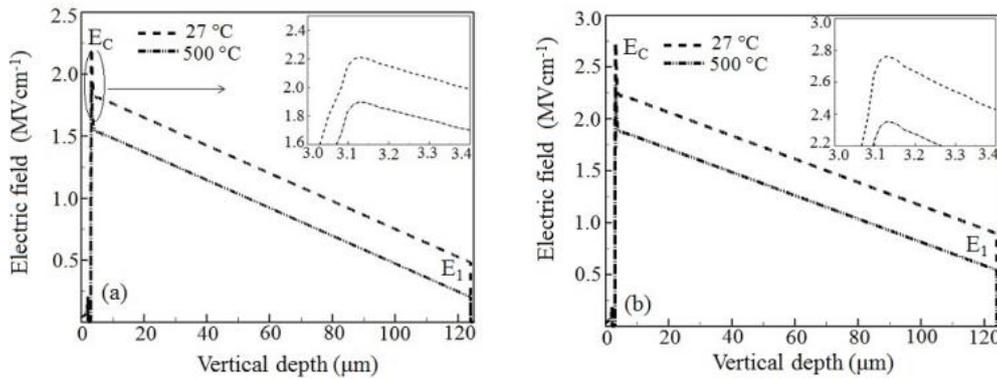


Fig. 4. Device depth dependent electric field distribution at room and high temperature of 500 °C for (a) 14 kV and (b) 19 kV of 4H-SiC VJFET.

From the above discussion, we can simulate the distribution of electron velocity throughout the entire depth from surface to drain region as shown in Figure 5. In general, the electric field has closely influenced the electron velocity. Therefore, an overshoot in velocity, due to high electric field, exists at the edge of the gate and reaches the saturation value as clear at point 1 [31]. As discussed in the previous section, the longitudinal field has significant effect underneath the gate. Although transverse electric field has low significant effect, superimposing with the longitudinal electric field can create the variation in velocity as clear at point 2. 19 kV design has stronger variation than 14 kV design. Therefore, the velocity approaches a high value of  $2.2 \times 10^7$  cm/sec and  $2.04 \times 10^7$  cm/sec for 19 kV and 14 kV design, respectively. Only low significant effect of transverse electric field was observed and the longitudinal electric field has stronger effect throughout the drift region. In the third zone, the velocity is constant, even with long drift layer thickness. The actual reason for constant velocity is the uniform electric field, due to constant low doping profile. It is noticeable that the increase in temperature increases the generation carrier and leads to a reduction in the electron velocity.

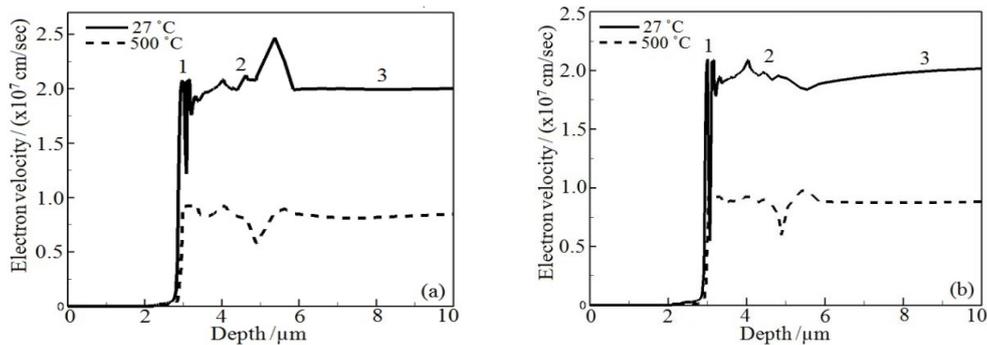


Fig. 5. Device depth dependent electron velocity distribution at room and high temperature of 500 °C for (a) 14 kV and (b) 19 kV of VJFET.

## 5. Conclusions

The breakdown voltage characteristics of the 4H-Si VJFET and its improvements have been presented. The influence of temperature has been demonstrated and results suggested the negative temperature coefficient for breakdown voltage. At  $N_{\text{gate}} = 5 \times 10^{17} \text{ cm}^{-3}$ , the range of breakdown voltages of 14 to 10.6 kV were simulated in the temperature range of 27 to 500 °C. The improved breakdown voltage of 19 kV was obtained when  $N_{\text{gate}} = 1 \times 10^{18} \text{ cm}^{-3}$ . Finite elements

simulation suggested that 27% of higher electric field is required for 19 kV when compared with 14 kV breakdown voltages.

This theoretical study has also led to consider the punch through behavior relevant to the electric field distribution based on the  $p^+n^-n^+$  structure. This mechanism can damage the drain contact due to presence of electric field at  $n^-n^+$  junction. Finally, 14 kV has shown good agreement with the reported experimental results. Finally, we suggest that the Lackner is a very good predictive model for the analysis of breakdown voltage characteristics of normally-off 4H-SiC VJFET.

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