FABRICATION OF THIN DIELECTRIC MEMBRANES FOR MICROWAVE APPLICATIONS

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This paper describes the fabrication technology for thin SiO_2/Si_3N_4 membranes on a silicon wafer substrate, with areas ranging from 0.9 mm^2 to 34 mm^2. The main challenges were the deposition of stress compensated dielectric films, uniform etching of the whole 4 inch wafer, while releasing the membranes and dicing the wafer in individual chips.

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1. Introduction

The idea of suspending microwave and millimeter-wave components on thin dielectric membranes was introduced in the early '90s in order to improve the performances by providing a propagation medium with the permittivity close to 1. Numerous structures were reported (filters, antennas, inductors etc.) fabricated using both silicon and GaAs micromachining [1]. A continuous effort has been spent on improving the mechanical stability and fabrication yield using different dielectric layer structures and micromachining techniques.

For example, in the case of standard on-chip planar antennas, the silicon substrate absorbs most of the radiation energy, leading to undesired substrate excitation modes and dielectric losses, which drastically affect the overall antenna efficiency and fractional bandwidth. In order to improve these parameters, it is necessary to remove the bulk silicon underneath the antenna by using advanced silicon micromachining techniques [2]. A cross-section, showing the layer configuration necessary for device fabrication, is shown in figure 1. The patterned metallization of the planar circuit supported by the dielectric membrane and the surrounding bulk silicon walls can be noticed.

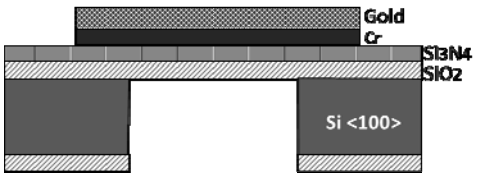

Fig. 1: Cross-section of the final structure (not at scale)

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The work presented in this paper describes the use of Inductively Coupled Plasma – Reactive Ion Etching (ICP-RIE) and Plasma Enhanced Chemical Vapor Deposition (PECVD) systems for the fabrication of thin SiO_2 / Si_3N_4 membranes with areas ranging from 0.9 mm x 1 mm to 5.56 mm x 6.1 mm on a silicon wafer substrate. The main challenges of the presented work were the deposition of stress free bi-layer dielectric films, back-etching of the silicon wafer to release the membranes and the dicing of individual chips.

2. Technological Approach

The silicon oxide grown in wet atmosphere at high temperatures exhibits residual compressive stress of -200 MPa to -300 MPa [3,4]. In order to compensate for the compressive stress of the oxide, the silicon nitride layer has to be deposited with an intrinsic tensile stress of a similar magnitude.

2.1 Silicon Nitride Deposition

The deposition of silicon nitride was performed on a 4", <100> orientation, low resistivity (1-10 Ohm•cm) silicon wafer having a thickness of 525µm, with a thermally grown oxide layer having a thickness of ~1.5 µm. Before the deposition of the nitride layer, the wafer is cleaned in a RCA1 solution ($NH_4OH:H_2O:H_2O_2$) for 30 minutes and spin dried. The Piranha solution was avoided to ensure the wafer is free of sulfur contaminants before the deposition of the nitride layer. The silicon nitride is deposited on the front side of the wafer in a Plasma Enhanced Chemical Vapor Deposition – PECVD system (LPX-CVD from SPTS) using a mixed frequency process. The mixed frequency process allows the compensation of stress in the nitride film by alternating layers having tensile stress and compressive stress. Mixing of High and Low frequency power allows control over ion bombardment and hence control over film stress and film density [5].

The deposition of silicon nitride takes place following the reaction of silane and ammonia: $SiH_4 + NH_3 > SiN_x + H_2$. Mechanical properties are significantly influenced by the deposition conditions, and can be considerably different from those of their bulk material counterpart [6]. The key deposition process parameters, like substrate temperature, gas composition, RF power and pressure, determine the mechanical parameters of the layer, as well as the deposition rate, layer uniformity and intrinsic stress.

2.2 Backside Deep Etching of the Silicon Substrate

The release of the membranes was performed from the backside of the wafer, using a Bosch Process in the ICP-RIE system Plasmalab100 from Oxford Instruments. The process uses a gas chopping technique allowing the etching of vertical walls. During this step, in order to avoid the use of the dicing blade for cutting individual chips, the dicing was performed at the same time. The masking layer included inter-chip lines which allowed the etching of the silicon substrate and releasing the individual chips at the end of the process. After 180 minutes, the etching was stopped and an additional dummy wafer was placed under the processed wafer to avoid wafer fracture along the inter-chip lines. The process continued until the SiO_2/SiN_x layer was reached.

The etching non-uniformity over the wafer was evaluated, and the full etching time was optimized to allow the release of as many membranes as possible without damaging or breaking them.

For this step, different masking layers were tested, to allow through etching of the substrate without affecting the bulk silicon walls that support the membranes (see Fig.1).

The final chips were carefully cleaned of residual photoresist in acetone and isopropyl alcohol, and were dried over a hot plate at 90^{o}C.

3. Results and Discussions

3.1 Silicon Nitride Deposition

The deposition process took place at 300^{o}C, using SiH_4 and NH_3 (1:1 ratio) as process gasses and N_2 as dilution gas. The ratio between the process gasses and the dilution gas was 1:24.5. The deposition pressure was kept constant at 900 mTorr. In order to reduce the stress in the

deposited silicon nitride layer, a mixed process was used, by alternating the high frequency (HF) and low frequency (LF) generators. The HF RF power was 30 W for 6 seconds followed by LF RF power of 35 W for 2 seconds. The obtained deposition rate was 25.6 nm/min. The total thickness of the deposited nitride film was measured by using the NanoCalc-XR refractometer. The non-uniformity of the deposited nitride layer was calculated by a 9-point mapping method. The measurements of the SiN_x layer, shown in Table 1, reveal a deposition non-uniformity of approximately 0.7%, and an average thickness of 309 nm.

Table 1. The thickness measurements of the oxide and nitride films measured in 9 points. The measurements are expressed in nanometers

Pt. no.	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
SiO_2	1532.5	1521.7	1518.9	1525.6	1539.3	1531.4	1520.9	1520.7	1524.9
SiN_x	310.8	311.5	309.4	307.6	302.2	310.6	310.7	308.1	306.6

Pressure is a critical parameter which greatly influences the characteristic of the SiN_x layer. Lower pressure results in an increase in electron energy, which subsequently leads to an increase in N to SiH_3 radical ratio, namely the decrease of Si/N ratio. Increasing the pressure leads to higher deposition rate and uniformity, but also induces more tensile stress in the layers. Our experiments show the process pressure of 900 mTorr would be optimal for SiN_x deposition due to its stable plasma and low residual stress generated.

The RF power levels determine the electron density, which in turn contribute to the ionization and dissociation rate of the process gasses. The power levels play an important role in determining the dominant film content. At high power, the concentration of N^* species in the process gas is greatly increased due to the high dissociation rate. This results in an increased incorporation of N bonding in the SiN_x film, which leads to a tendency of volume expansion of the SiN_x, in order to reach steady state. Thus, higher RF power generates a high compressive stress. The deposition in HF mode (13.56 Hz), at low power (30 W), generates a tensile stress in the range of 140 MPa [7]. For the LF deposition mode (380 kHz), the intrinsic stress state of the silicon nitride layer is compressive. The main reason is that at high frequency (13.56 MHz) only the electrons are able to follow the RF field while the ions are "frozen" in place by their heavier mass. In LF mode the ion bombardment is significantly higher, which not only enhances chemical reactions but also causes a slight etching of the film and leads to a change of the stress state from tensile to compressive.

3.2 Masking Layer for the Deep Reactive Ion Etching Process

The deep reactive ion etching requires a masking layer strong enough to last the entire process. The Bosch process etches the thermal SiO_2 at a rate 13 nm/min. The 1.5 μm thick thermal oxide on the back of the wafer would last for only 110 minutes, not sufficient to last the entire process, thus requiring an additional masking layer. As the standard photolithographic masking layers were not strong enough, several additional masking layers were investigated.

A 3μm thick PECVD SiO_x was deposited from a liquid TEOS source to complement the masking layer. Our tests have shown that the Bosch process etches this deposited SiO_x at a rate of 15 nm/min. The total 4.5 μm SiO_2/SiO_x masking layer has proven thick enough to last a 300 minutes process, enough for the membranes to be released safely.

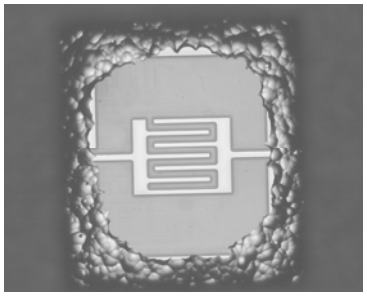

Fig. 2: Optical photo of a membrane supported structure seen from the back-side.
(The white lines are the Cr/Au metallization pattern)

Figure 2 shows a membrane released with a SiO_2/SiO_x masking layer seen from the back-side. The side walls of the etch-through are clearly not vertical, and have a very rough aspect. This is due to the undercutting of the oxide masking layer during patterning, leading to an uneven thickness of the masking layer near the margins.

Another layer tested for the etching mask was the AZ-4562 photoresist. The main advantages of this photoresist are the maximum thicknesses of 6.2 μm and the slower etch rate. Our tests showed that the Bosch process etches it at a rate of 35 nm/min, making it the optimal candidate for releasing the membranes.

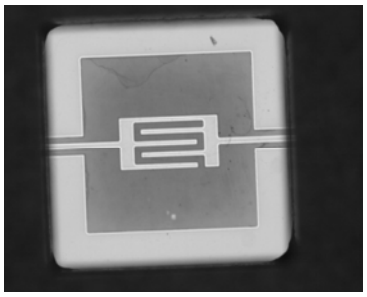

Fig 3: Optical photo of a membrane supported structure seen from the back-side
(the white lines are the Cr/Au metallization pattern)

Figure 3 shows a membrane released with a SiO_2/AZ-4562 masking layer seen from the back-side. The side walls of the etch-through are clearly vertical, with a smooth aspect.

3.3 Deep Reactive Ion Etching Process and Release of the Membranes

One of the main goals is to obtain the individual chip dicing at the same time with the membranes themselves, in order to avoid the use of a dicing blade, which might damage the thin membranes due to vibrations and water cooling process. For this purpose, alongside the membranes, inter-chip lines were also patterned on the masking layers. Figure 4 presents the layout of the membranes and inter-chip lines. The main problem was the Helium backpressure, which is applied on the bottom-side of the wafer to allow quick cooling. During the Bosch process, due to the additional pressure from the Helium cooling, the wafers would crack along the inter-chip lines as they are etched deeper. In order to prevent this, we decided to use a dummy wafer, placed between the processed wafer and the substrate electrode.

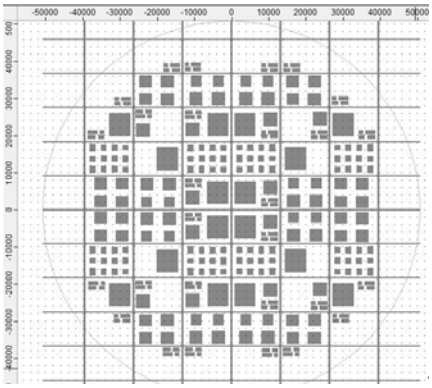

Fig. 4: Layout of the photolithographic mask for patterning the membranes and inter-chip lines. The dimensions are expressed in micrometers

By introducing the dummy wafer, the heat building up on the processed wafer could not be efficiently removed, and during long processes it caused damage to the Cr/Au metal patterning defining the microwave and millimeter wave circuits. In order to remove heat efficiently, normally a thermal conducting thin layer is applied between the dummy and the processed wafer, which is later removed by acetone. Because this layer is in direct contact with the membranes, the acetone cleaning causes them to break. Thus, we avoided the use of any intermediary layer and placed the processed wafer directly on the dummy wafer. In order to avoid temperature build up during the long process, we opted for a multiple steps etching.

During the first step, the processed wafer is placed directly on the lower electrode and etched for 180 minutes, etching approximately 400 μm of the bulk silicon. Also, a depth mapping of the wafer is done, to evaluate the etch depth and uniformity. The measurements revealed an etch non-uniformity of ~4%. The membranes close to the edge of the wafer were etched for 415 μm, while the membranes close to the center of the wafer were etched for only 390 μm, as shown in figure 5.

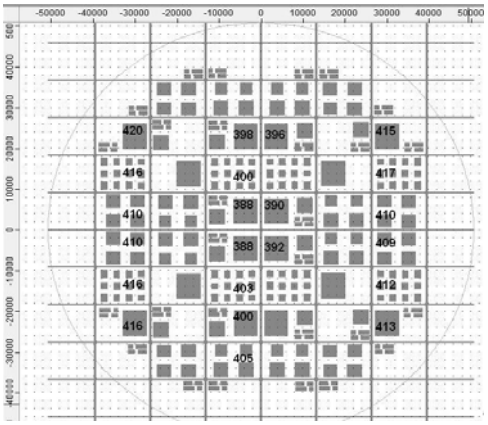

Fig 5: Etched depths mapped after 180 minutes of processing

The subsequent steps were short etching steps of 30 and 15 minutes. The short plasma exposures were necessary to allow the wafer to cool down during the etching, and also allowed us to verify the etching rate and adjust the timing correctly. After these steps, the membranes placed at the margins of the wafers were clearly visible. The process continued with short 3 minute steps until most of the membranes were completely released. Due to the etch non-uniformity, the central membranes were not fully released, as seen in figure 6.

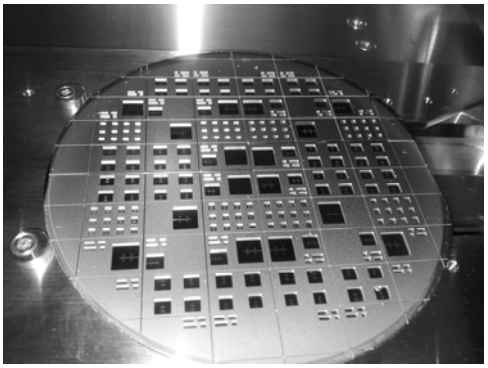

Fig. 6: The processed wafer, placed on top of the dummy wafer at the end of the etching process

After the membranes are released, the wafer is left overnight in a dish with acetone to remove any traces of photoresist. At this stage, the individual chips, being held together only by the thin SiO_2/SiN_x layers, can be easily separated from the rest of the wafer. Each chip is then rinsed in isopropyl alcohol and dried over a hot plate at 90^{o}C.

4. Conclusions

A technological process for fabricating robust SiO_2/SiN_x membranes has been successfully designed and implemented. Several microwave and millimeter wave structures, patterned on a 1 μm thick Cr/Au layer deposited on top of the double dielectric layer, were used as test vehicles and showed good results for frequencies up to 220 GHz. The proposed technological process completely eliminates the use of blade dicing which can cause significant damage to the structures due to water cooling and vibrations.

The double dielectric layer was fabricated with reduced stress to prevent the cracking or deformation of the membranes. The compressive stress in the grown SiO_2 was compensated by a thin layer of PECVD deposited SiN_x, using the mixed frequency mode. The deposition parameters were optimized to reduce the overall stress.

The membranes were released by deep ICP-RIE of a 525 μm thick silicon wafer. The etch process showed a 4% etching non-uniformity across the wafer, thus the membranes closer to the edge of the wafer were released earlier than the ones closer to the center. Any attempts to fully release the central membranes led to defects in the previously released ones. Several masking layers were tested for optimized results.

The dicing of the individual chips was performed at the same time with the etching of the bulk silicon, by patterning inter-chip lines alongside the membranes.

Acknowledgments

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References

[1] A. Muller, D. Neculoiu, R. Plana, G. Konstantinidis, Wireless Technologies, CRC Press (2007).

[2] A.-C. Bunea, D. Neculoiu, A. Avram, T. Kiuru, T. Vaha-Heikkila, A. Takacs, P. Calmon, presented at 2012 Asia-Pacific Microwave Conference Proceedings (APMC), 4-7 Dec. 2012, Kaohsiung, Taiwan.

[3] J. T. Fitch, G. Lucovsky, E. Kobeda, and E. A. Irene, J. Vac. Sci. Technol. B **7**, 153 (1989).

[4] E. Kobeda and E. A. Irene, J. Vac. Sci. Technol. B **4**, 720 (1986).
[5] Poh Lam Ong, Jiashen Wei, Francis E H Tay and Ciprian Iliescu, J. Phys.: Conf. Ser. **34**, 764 (2006).
[6] H. Huang, K.J. Winchester, Y. Liu, X.Z. Hu, C.A. Musca, J.M. Dell, L. Faraone, J. Micromech. Microeng. **15**, 608 (2005).
[7] C. Iliescu, M. Avram, B. Chen, A. Popescu, V. Dumitrescu, D.P. Poenar, A. Sterian, D. Vrtacnik, S. Amon, P. Sterian, J. Optoelectron. Adv. Mater. **13**, 4, (2011).