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MORPHOLOGICAL AND ELECTRICAL STUDIES OF Zn DOPED CdTe THIN FILM BY STACKED ELEMENTAL LAYER METHOD

S. SHANMUGAN*, D. MUTHARASU
Nano Optoelectronics Research Laboratory, School of Physics, Universiti Sains Malaysia (USM), 11800, Penang, Malaysia

Zn doped CdTe thin films have been prepared by using Stacked Elemental Layer (SEL) method. The electrical studies of the annealed thin films have been carried out for different temperature using Van der Pauw technique. The conductivity of Zn doped film lies in between 6.9×10^{-4} to 1.56×10^{2} Scm^{-2}. The effects of annealing temperature on morphology were performed by using Scanning Electron Microscope (SEM) and analyzed by using *imageJ* software. Annealed films are having nano size particles of about 26 nm. An EDAX spectrum reveals the prepared thin films having the desired composition.

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1. Introduction

The semiconductor alloy, $Cd_{1-x}Zn_xTe$, is a good candidate for the top cell in tandom solar cell structure since the energy gap is tunable over a wide spectral range from visible (2.3 eV) to near infrared (1.5 eV) by changing Cd and Zn composition. For these applications, utilization of CdZnTe layers grown on GaAs substrates is the most practical approach, since layers with large area can be grown on low-cost and robust substrates.

It has merits as a top cell material in that it has complete miscibility, it is isostructural and isoelectronic to CdTe, p-type, and chemically stable material [1]. However, few attempts have been made to grow these films in polycrystalline form and even fewer studies have been reported about post deposition treatments [2–6]; hence, little is known about the electronic properties of such films.

In fact p-ZnTe/i-CdTe/n-CdS solar cells were fabricated by different authors [7,8] using sequential metalorganic vapour phase epitaxy of ZnTe and CdTe layers on CdS substrats, and obtained cell efficiencies up to 13%, under air mass one (AM1) illumination. This led to an increasing interest in the development of wide band gap absorbers based on the alloys of ZnTe and CdTe, with a variety of advantageous properties.

SEL technique was originally developed to produce CuInSe2 thin films [9]. But it has also been used to produce CdTe films [10,11]. It is particularly suitable for deposition of compound semiconductor films, as it provides good control of composition; also, it seems to be a promising method for producing highly efficient CdTe/CdS solar cells [11].

In this paper, we report on Zn doped CdTe thin films grown by the Stacked Elemental Layer technique. The influences of the temperature were analyzed on surface properties, grain growth and conductivity of the annealed samples and also discussed the change in the morphological nature. In our knowledge, this kind of work has not been reported elsewhere.

*Corresponding author: subashanmugan@gmail.com

2. Experimental work

Zn doped CdTe thin film has been prepared at room temperature by SEL method using PVD unit (model BC 300). The 5N purity Te, Sb and Cd powders were used for film preparation. Sequential layer of Te, Cd followed by Zn were coated on soda lime glass slides. The deposition rate of 3Å/s and 1.5Å/s was maintained for Cd & Te and Zn films respectively. To achieve the desired stoichiometry, the thickness of the elemental layer (Te, Zn and Cd) was adjusted. The ratio of the thickness of elemental layers were fixed as t_{Te} / t_{Cd} = 1.5318 (Te & Cd) and t_{Te}/t_{Zn} = 1.9513 (Zn) and the thickness of Te, Zn and Cd elemental layers were maintained at 400nm, 27nm and 214nm respectively for 15% of Zn doping. The distance between the substrate and source was fixed at 10 cm. To enhance the film uniformity, rotary drive assembly has been used.

The stacked layer of Te/Cd/Te/Zn/Cd was allowed to isothermal annealing for 500°C for different time (60, 90 and 120min) in Ar gas atmosphere in a separate vacuum furnace. The electrical properties were carried out using vader paw technique for different temperature and the results were analyzed. The morphological nature of the annealed thin film has been studied using SEM and also the compositional analysis was studied using EDAX. *ImageJ* software has been used to analyze the grain size and morphology of the annealed thin films.

3. Results and discussion

3.1 Morphological Studies

Morphological nature of the synthesized film for different annealing time were analyzed by using Scanning Electron Microscope and presented in Fig.1-3. The figures reveal that the considerable morphological change could be observed as the annealing time increases. It could be observed that the influence of annealing time on the morphology of the stacked film and also the modification due to the diffusion of Zn and reaction with Cd and Te were observed. The SEM image also shows the white particles on the surface of annealed film due to the presence of Cd elements which are not diffused by the annealing process. Fig.1B, 2B and 3B show the 3D image of the surface of the stack after annealing plotted by using ImageJ software. It reveals the formation of smoothened surface at higher annealing temperature with high annealing time. Obviously, the surface roughness of the synthesized film was low and It could be seen in the 3D image.

By using the software, the average grain size of each samples have been evaluated and plotted with annealing temperature are shown in Fig.4. It could be observed the reduction in the particle size as the annealing time increases from 60 min to 120 min.

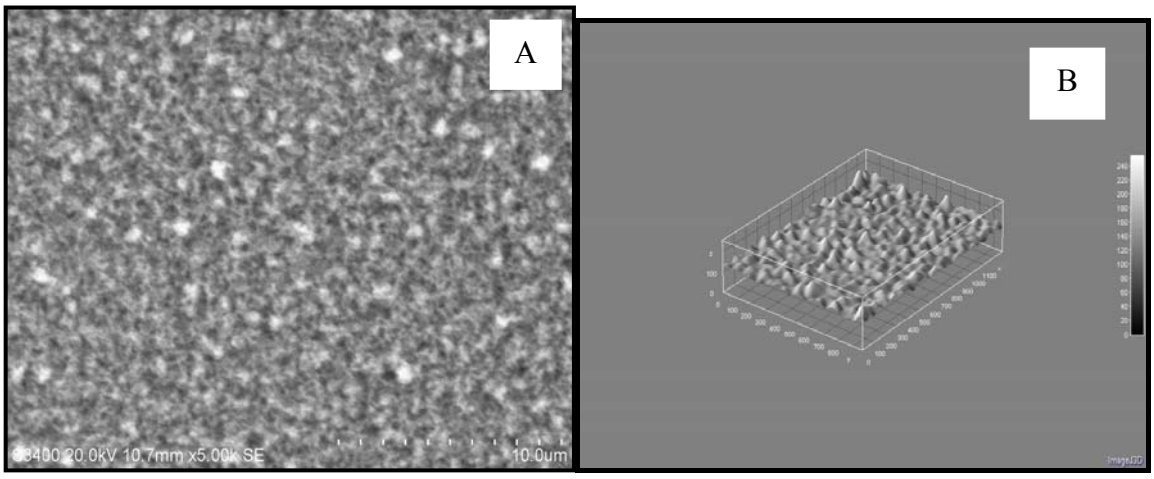

Fig.1 (A) Surface of 15% Zn doped CdTe thin film (annealing temperature 500°C for 60min (B)3D image of surface of annealed film at 500°C for 60min

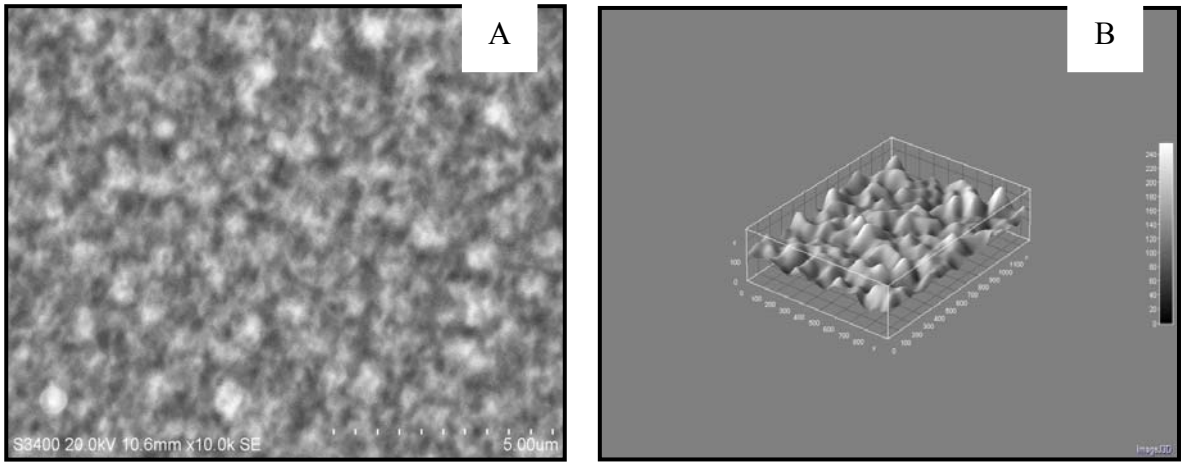

Fig.2 (A) Surface of 15% Zn doped CdTe thin film (annealing temperature 500°C for 90min (B)3D image of surface of annealed film at 500°C for 90min

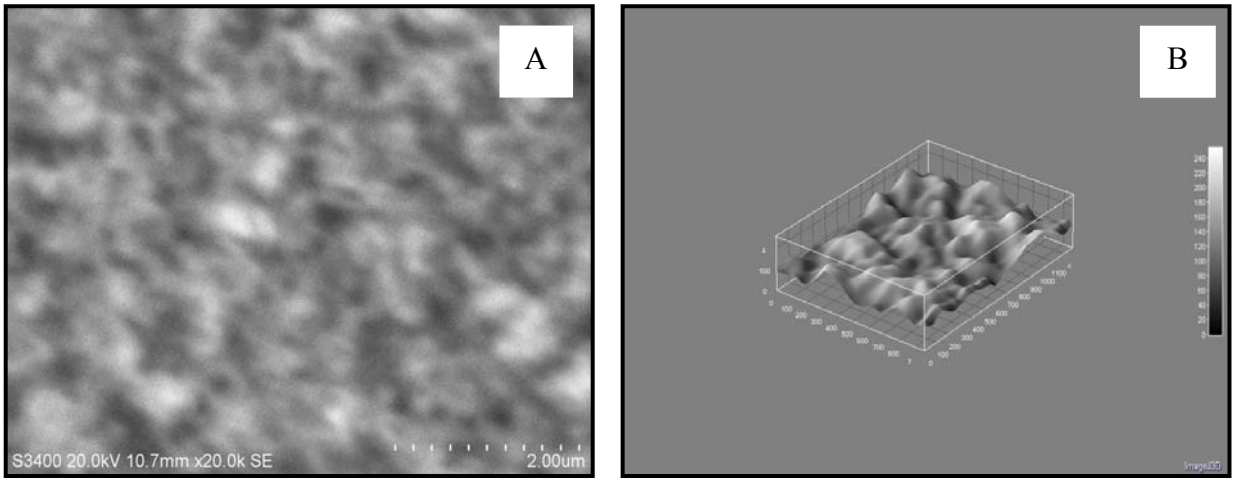

Fig.3 (A) Surface of 15% Zn doped CdTe thin film (annealing temperature 500°C for 120min (B)3D image of surface of annealed film at 500°C for 120min

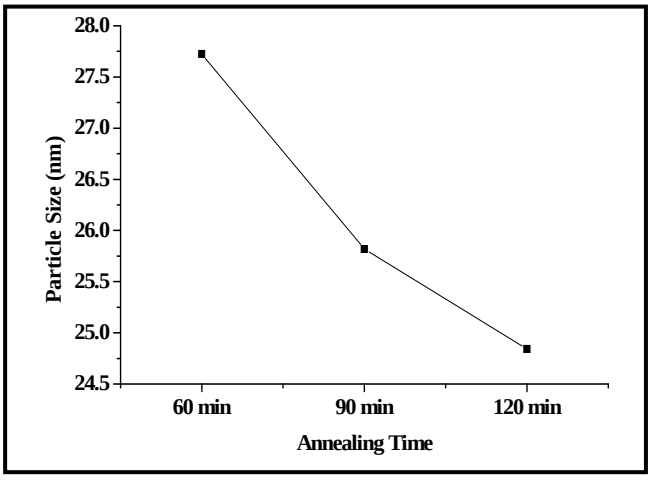

Fig.4. Variation of Particle size for different annealing time

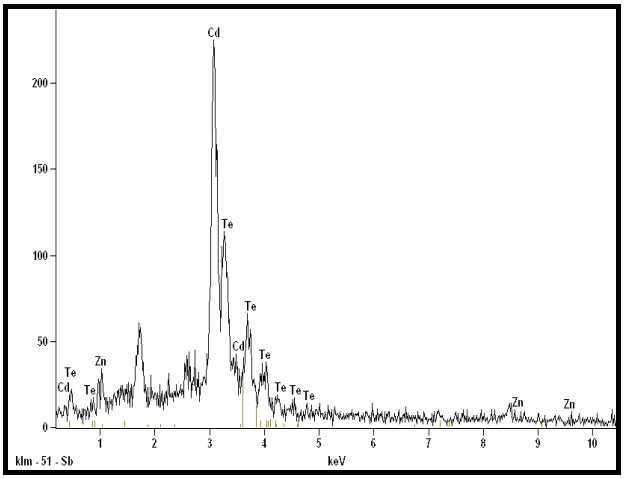

Fig.5. EDAX spectrum of Zn doped CdTe thin film annealed at 500°C for 60 min.

Table 1. Composition of 15% of Zn doped CdTe thin film annealed at 500°C for 60 min

Element present	Atomic %
Cd	71.09
Te	21.70
Zn	7.21

EDAX spectrum of Zn doped CdTe thin film annealed at 500°C for 60 min were recorded are shown in Fig.9 and the atomic percentage of the elements are tabulated in Table – 1. The EDS spectrum shows only the presence of Cd, Te and Zn. It shows the expected Zn composition is presented in the annealed film. As the annealing of the stack, the atomic percentage of Cd, Te and Zn may vary as the annealing time increases due to the diffusion and reaction with other elements (Cd and Te). But it would not exceed the desired stochiometry. From these results, it is suggested that the CdZnTe alloy may present in the annealed stack.

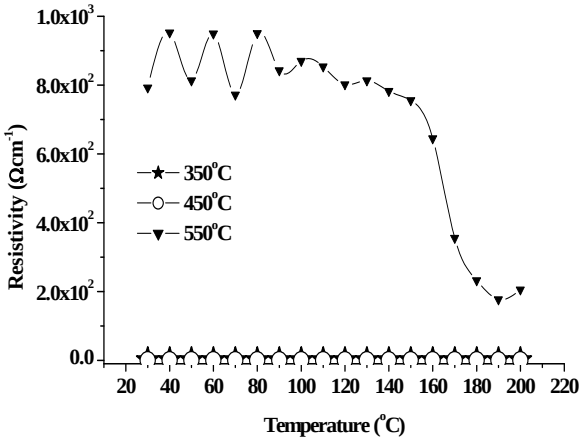

Fig.6. Resistivity Vs Temp. of Zn doped CdTe thin film

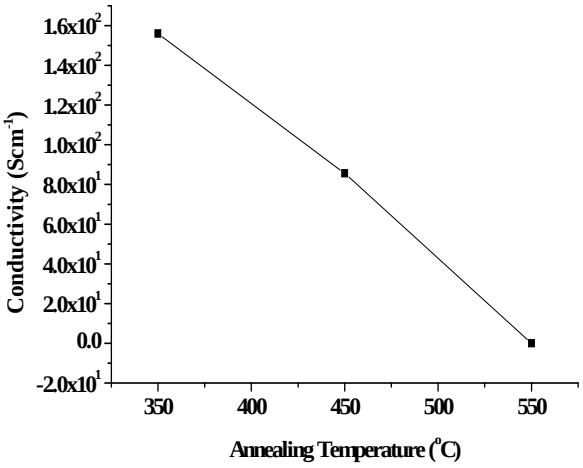

Fig.7. Variation of conductivity vs temperature of Zn doped CdTe thin film by SEL method

3.2 Electrical studies

The resistivity of the Zn doped CdTe thin films have been measured by using vander paw technique. The semiconductor behavior of the annealed stack have been proved by performing the resistivity measurements with temperature are presented in Fig.6 and reveals that the annealed stack at high temperature ie 500°C for 60 min shows the semiconductor behavior as the resistivity decreases with increasing temperature.

It shows the resistivity of films treated at 350°C and 450°C are very low ($1x10^{-2}\Omega cm^2$) reveals the metallic behavior since the surface of the film covered with traces of non reacted Cd atoms in the annealed stack (Te/Cd/Te/Zn/Cd) already stated in the SEM analysis.

As the temperature increases, free elements undergo thermal reaction by diffusion process and get conversion as the compounds like CdTe, ZnTe and CdZnTe. This process reflects the decreased conductivity at high temperature and possibility for making the mixed alloy like CdZnTe and ZnTe over the surface (See fig.7.) This type of results has been observed first time by using these materials by SEL method.

As conclude, the annealed stack with high temperature having the conductivity lies between 6.9×10^{-4} to 1.56×10^{2} Scm^{-2}.

4. Conclusion

Stacked Elemental Layer method have been used for the synthesis of (15%) Zn doped CdTe thin film. SEM analysis was performed and showed the significance of annealing time for the elemental stack on grain growth and surface morphology. It is observed that the small variation on particle size of the synthesized films. The atomic percentage of elements presented in the stacked film has been measured by EDAX spectrum and reveals the presence of free Cd on the surface. The influence of heat on the electrical properties of stacked layer has been analyzed by the resistivity measurements. The Zn incorporation enhances the conductivity of the annealed stack at higher temperature shows the effective doping by SEL method.

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