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TEMPLATE SYNTHESIS OF Cu-Se HETERO-JUNCTIONS USING ANODIC ALUMINA MEMBRANE AND THEIR CHARACTERIZATION

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It is well known that template synthesis is a simple and versatile method for preparing nanostructures within the pores of a microporous template membrane. Due to their uniform and nearly parallel porous structures, anodic alumina membranes (AAM) have become ideal templates for the electrochemical deposition of the highly anisotropic, aligned nanowire arrays. Commercial anodic alumina membrane (Anodisc 25, Whatman, UK) having an average pore diameter of 200 nm, a nominal thickness of 60 µm and a pore density of 10^9 pores/cm^2, was used as a template. In the present study, template synthesis of Cu-Se hetero-junctions has been achieved in an electrochemical cell fabricated in our laboratory. The electrolytes used had a composition of 200 gm/l $Cu\ S0_4.5H_2O$ + 25% of dilute H_2S0_4 for deposition of Copper and a composition of SeO_2 (8×10^{-4} M) with 0.5 ml of 35% dilute H_2SO_4 for deposition of Selenium, the inter-electrode distance was kept 0.5 cm and a dc source was used for electrodeposition at room temperature. The Cu-Se nanowires were liberated from the host matrix by keeping AAM immersed in 1 M NaOH for 1hour. SEM images of fabricated hetero-junctions reveal a parallel alignment with approximately equal wire length. Chemical composition is determined using Energy Dispersive X-ray Spectroscopy (EDS) and the spectrum reveals that Cu-Se hetero-structures are composed of Cu and Se metals with appropriate stoichiometry. I-V characteristics of Cu-Se hetero-junctions have been investigated using Keithley Model 4200 SCS programmable dual source meter.

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1. Introduction

Template synthesis is an elegant chemical approach for the fabrication of nanostructures. A variety of nano-wire arrays have been obtained by filling a porous template that contains a large number of cylindrical holes with a narrow size distribution. Electrochemical deposition [1-4] or other chemical methods [5] are used for filling up cylindrical holes with a desirable metal or semiconductor in solution form.

Commercially available templates are anodic alumina membrane (AAM) and track etched membrane (TEM) which are most commonly used. Other membranes have also been used, such as nanochannel array on glass [6], meso-porous materials[7], porous silicon by electrochemical etching of silicon wafer [8], zeolites [9] and carbon nano-tubes [10]. Pore sizes range from 10 nm to 100 µm in commercial templates and pore densities can be as low as 1 pore/cm^2 and as high as 10^9 pores/cm^2. Template materials should be chemically and thermally inert during synthesis, depositing material or solution must wet the internal pore walls and it should behave as an insulator in case of electrodeposition [11].

Historically, the method of template synthesis was introduced by Possin [2] who prepared different metallic wires with diameters as small as 40 nm in pores of mica TEM. It has been exploited in India by author's group [12, 13] during 90s and by other groups during recent years [14-17]. Applications of template synthesis [18] include arrays of electron field emitters, biosensors, novel magnetic disk materials, magnetic sensors, anisotropic optical filters and other nano-devices. In the present study, template synthesis of Cu-Se hetero-junctions has been achieved in an electrochemical cell fabricated in our laboratory. The morphology of Cu-Se heterojunctions is revealed by Scanning Electron Microscope (SEM) at PU, Chandigarh and the elemental composition of metallic copper and semiconductor selenium has been determined using Energy Dispersive X-ray Spectroscopy (EDS) facility available at PAU, Ludhiana.

2. Experimental Technique

Electrodeposition technique used in our experiment is identical in principle to that used for the electroplating process. Commercial anodic alumina membrane (Anodisc 25, Whatman, UK) having an average pore diameter of 200 nm, a nominal thickness of 60 µm and a pore density of 10^9 pores/cm^2, was used as a template. Prior to the electro-deposition process, a thin film of copper (0.5 µm) was sputtered onto one side of anodisc and subsequently reinforced galvano-statically with copper. This metal layer provides a stable substrate for the growth of hetero-junctions.

All the chemicals used were RA grade (purity 99.9% Loba Chemicals) and all solutions were prepared in de-ionised water. Electrochemical cell used for synthesis of Cu-Se hetero-junctions was fabricated in our laboratory [19]. A copper rod of 1 cm diameter tapered at the end was used as a sacrificial electrode (anode). The cathode consists of copper foil attached to anodisc by an adhesive tape of good conductivity. The electrolyte used had a composition of 200 gm/l Cu $S0_4.5H_2O$ + 25% of dilute H_2S0_4 at room temperature, the inter-electrode distance was kept 0.5 cm and a potential difference of 2V was applied for 10 min using a dc source. During the deposition process, we recorded the electrical current as a function of time. A typical chrono-amperometric curve [20] is obtained. When the anodisc pores were approximately half-filled up with copper metal, the electrolyte was drained out and a second electrolyte having a composition of SeO_2 (8×10^{-4} M) with 0.5 ml of 35% dilute H_2SO_4 was introduced. A potential difference of 1V was applied for 15 min. at 60^{o}C to electro-deposit Se semiconductor over Cu metal already deposited in pores. After the electro-deposition was over, the electrolyte was drained out and the cathode was rinsed with high purity water and ethanol. The filled template with copper backing was immersed in 1N NaOH for 1h to dissolve AAM completely and to liberate the Cu-Se hetero-junctions in the shape of nano-wires.

3. Results and discussion

The dried hetero-junctions of Cu-Se grown on 25 mm diameter AAM are cut into 2 pieces for their characterization. One piece is mounted on specially designed aluminum stubs with the help of double adhesive tape and coated with a layer of gold palladium alloy in JEOL Fine Sputter JFC 1100. It is viewed under JEOL JSM 6100 Scanning Electron Microscope (SEM) at an accelerating voltage of 20 kV. The morphology of Cu-Se hetero-junctions is revealed as shown in Fig.1 (a, b). The dimensions of Cu-Se hetero-junctions are consistent with the pore dimensions of AAM. SEM images of fabricated hetero-junctions reveal a parallel alignment with approximately equal wire length. During dissolution of AAM, some nanowires (hetero-junctions) get twisted or broken (Fig. 1c).

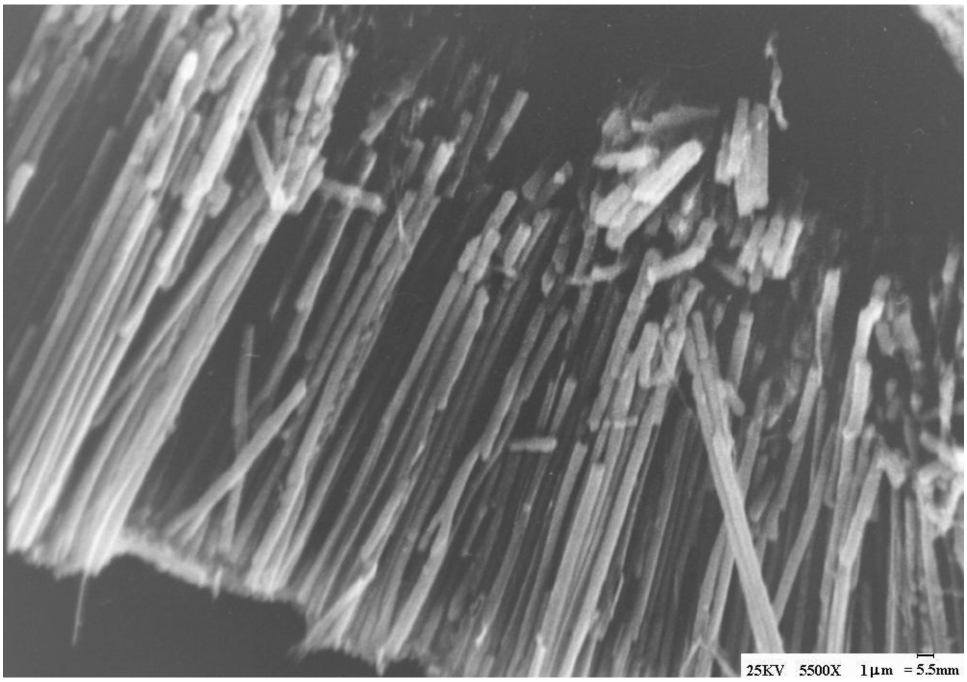

Fig. 1(a). SEM micrograph showing morphology of Cu-Se heterojunctions

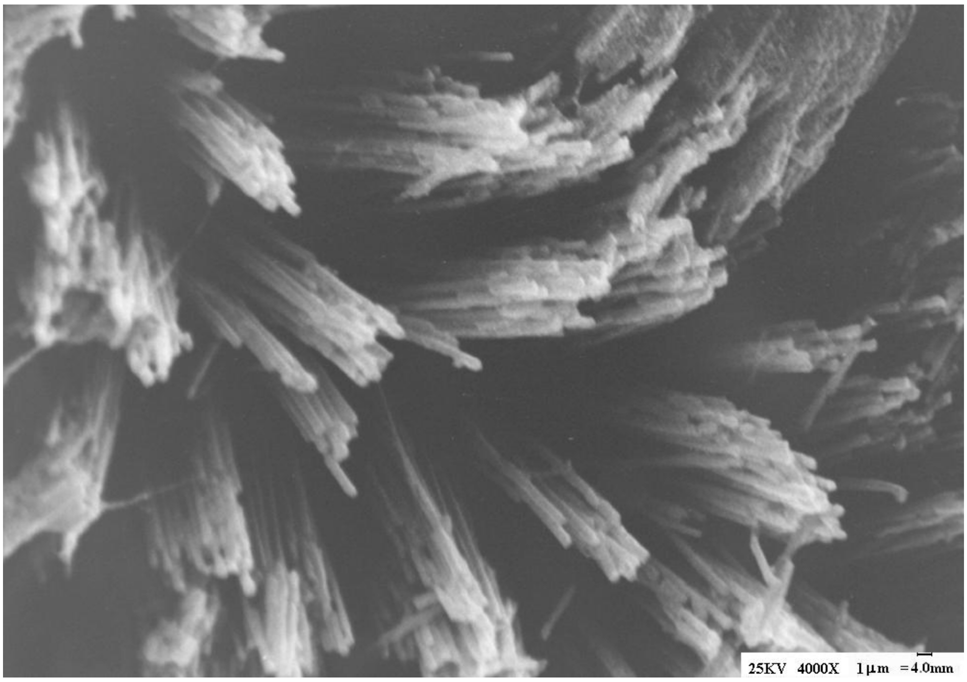

Fig. 1(b). Cross-sectional view of Cu-Se heterojunction bundles

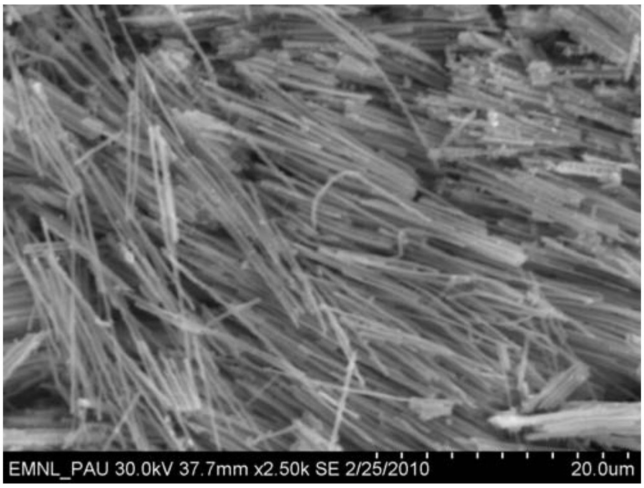

Fig.1(c) SEM micrograph of Cu-Se nanowires

For the quantitative compositional analysis, the second portion of liberated Cu-Se hetero-junctions was used. Chemical composition is determined using Energy Dispersive X-ray Spectroscopy (EDS) facility at PAU, Ludhiana. EDS spectrum (Fig.2) reveals that Cu-Se hetero-structures are composed of mainly Cu and Se metals. There are also peaks corresponding to elemental composition represented by C, O and Au. The prominent peaks are represented by Cu and Se and the Au peak occurs due to the gold sputtering of Cu-Se heterostructures.

Table 1 represents the elemental composition of Cu-Se heterojunctions. The stoichiometry of Cu-Se is almost 1:1 by weight % composition. The atomic % composition of all the elements is summarized in Table 1. Carbon atoms have highest atomic % composition which is quite unusual. It may be concluded that template synthesis using AAM is an efficient tool for fabrication of Cu-Se heterojunctions of pre-determined morphology and stiochiometry.

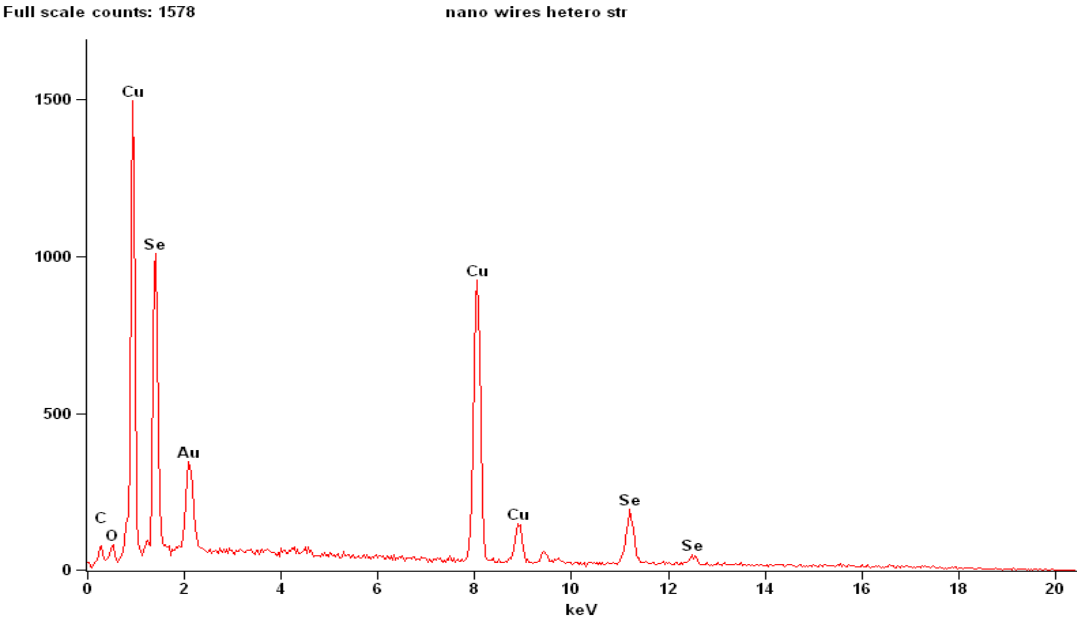

Fig.2. EDS spectrum showing elemental composition of Cu-Se heterostructures

Table 1. Elemental composition of Cu-Se heterostructures.

Element	***Net Counts***	***Net Counts Error***	***Weight %***	***Atom %***
C	360	+/- 28	9.55	38.14
O	302	+/- 58	1.09	3.26
Cu	15459	+/- 252	43.05	32.48
Se	3182	+/- 186	40.83	24.79
Au	530	+/- 100	5.48	1.33
Total			100.00	100.00

I-V characteristics of Cu-Se/ CdSe heterojunctions have been studied by some groups in India [14-16] to determine resonant tunneling diode behaviour of fabricated devices/junctions. We failed to observe such behaviour during our investigations. A prominent feature of I-V plot (Fig. 3) is a smooth curve showing increase of current with increase of voltage, in both forward and reverse bias modes. We can attribute this behaviour to Se semiconductor acting as a p-n junction diode but not to a resonant tunneling diode (RTD).

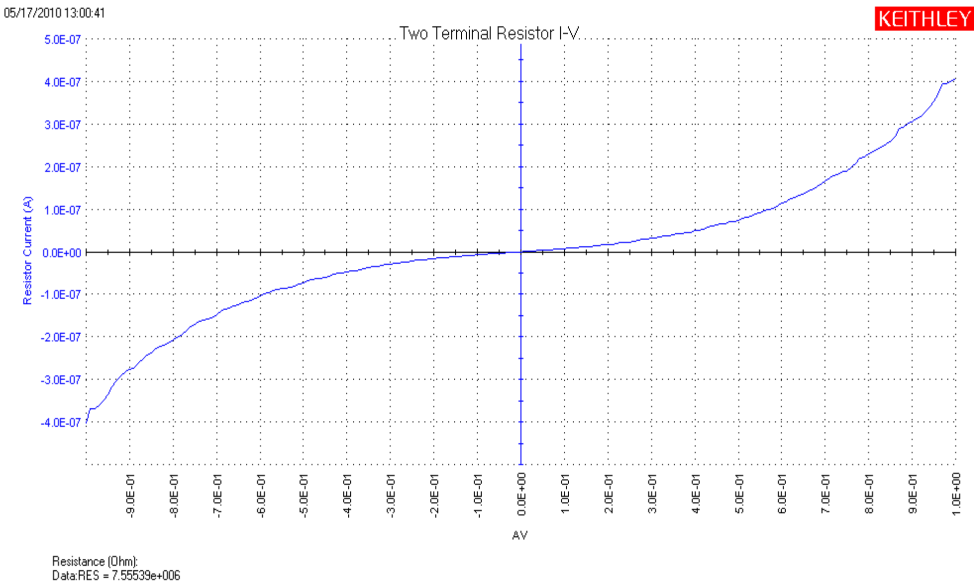

Fig. 3 I-V Plot of Cu-Se hetero-junctions/nanowires

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