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THIN-FILM p-type ZnTe TRANSISTORS BY PHOTOLITHOGRAPHY

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In this work, we built thin-film transistors, (TFTs), with a thickness of 75 nm of p-type ZnTe by photolithography. The paths were doped at 15 mg of CuN_2O_6-$3H_2O$ before depositing the contacts of Au and Ni to build source-drain of the TFTs. (I_D-V_D) curves were measured at different gate voltages, V_G and we had approximate value of the threshold voltage and mobility.

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1. Introduction

Since the appearance of the first functional TFT a-Si amorphous silicon in 1979 has been a breakthrough in display technology. The a-Si TFT is mainly used in flat screen displays and they can be built with a large, low cost and good resolution [1, 2]. There are also reports of a-Si TFTs in integrated circuits; however, the switching speed is slow for practical applications because the electron mobility, μ, is < 1 cm^2/Vs [3-5]. Another application is integrated image sensors (image sensors integrated) [6]. A new range of materials have been studied as an alternative to a-Si TFT, such as organic TFTs or OTFTs, which have a channel-type p. These OTFTs can be fabricated at room temperature without vacuum. Some of these semiconductors have mobilities higher than those of a-Si:H. However, to achieve good characteristics the OTFT, organic molecules need to be aligned in the interface, and few defects grain form, those are difficult. Currently, they are made OTFTs with small molecules such as pentacene and have better characteristics than the polymers of large molecules [7]. In these days, there is great interest in TFTs based on oxide semiconductors such as ZnO and In-Ga-Zn-O (IGZO) deposited by sputtering, the latter has a mobility of a higher order than the a-Si TFT: H and this mobility is sufficient for applications in integrated circuits. The problem with oxide-based TFTs are that they are sensitive to humidity, atmospheric, light and storage time. Therefore, replacing the TFTs of a-Si: H TFTs oxide for pixels in large-area LCD panels will be a challenge [8]. The first TFT p-type ZnTe was published by thermal evaporation [9] and PLD [10]. In this paper TFTs were built with 75 nm of ZnTe deposited by PLD. In the photolithography process routes were doped source-drain pathways of the TFT with 15 mg of CuN_2O_6-$3H_2O$ to make ohmic contact between the ZnTe and Ni and Au contacts.

2. Experimental

Thin-film transistors, TFTs of p-type ZnTe were built by photolithography using five masks. First, layers of Au(100 nm)/Cr(10 nm) were deposited on 500 nm of SiO_2 by Temescal

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1800 e-beam Evaporator. For gate metal patterning, the wafers were covered with positive photoresist, spin them at 2000 rpm for 60 seconds and heated at 115 °C for 90 seconds on CEE Spin Coater/Hotplate Operation. Then, the samples were exposed with a UV light with a dose of 130 mJ using the mask 1 (metal patterning) in Karl Suss MA6 BA6 Contact Aligner/Printer. After that, the exposed photoresist was developed using MF-319. Over the gate metal, a layer of 30 nm of HfO_2 was deposited by ALD, and 75 nm of p-type ZnTe by Pulsed-laser Deposition with excimer laser (KrF, λ = 248 nm) at an energy density of 0.78 mJ/cm^2. Then, 500 nm of parylene were deposited by SCS Parylene Deposition. As in the first step, the wafers were covered with photoresist to protect the TFTs channel using the Semiconductor and Hard-Mask Pattering (mask 2). One time that the channel was protected, the parylene layer and ZnTe film were removed using oxygen plasma with 100 mT of pressure with 50 watts of power for 8 minutes for the first and H_3PO_4 : H_2O_2 : H_2O = 1 : 1 : 20 for 30 seconds for the semiconductor. Next, a Gate Dielectric Pattering (mask 3) was used to remove the HfO_2 over Au gate contact with Buffered Oxide Etch (BOE 7:1) for 12 minutes. Before depositing the contacts, the pathways or lines of ZnTe were doped with Cu using Hard-Mask Pathways (mask 4). A solution with 15 mg of CuN_2O_6-$3H_2O$ was dissolved in 150 ml DI water, then, shaked in ultrasonic bath for 4 minutes and heated at 60 °C on a hot plate. Then, the sample with TFTs was immersed for 60 seconds, rinsed with DI water and dried with N_2 gas. Afterwards, the sample was annealed at 300 °C for 10 minutes in N_2 atmosphere. Soon, layers of Ni(10 nm) and Au(100 nm) were deposited over the doped pathways to have ohmic contact between the ZnTe and the contacts. For the source-drain patterning were used a concentration of (gold etch: H_2O = 1: 10) for 2 minutes and nickel etch for 8 minutes. In fig. 1 and 2 are showed a top view by optical microscopy and cross section, respectively. The width and length analyzed were W/L = 40/40

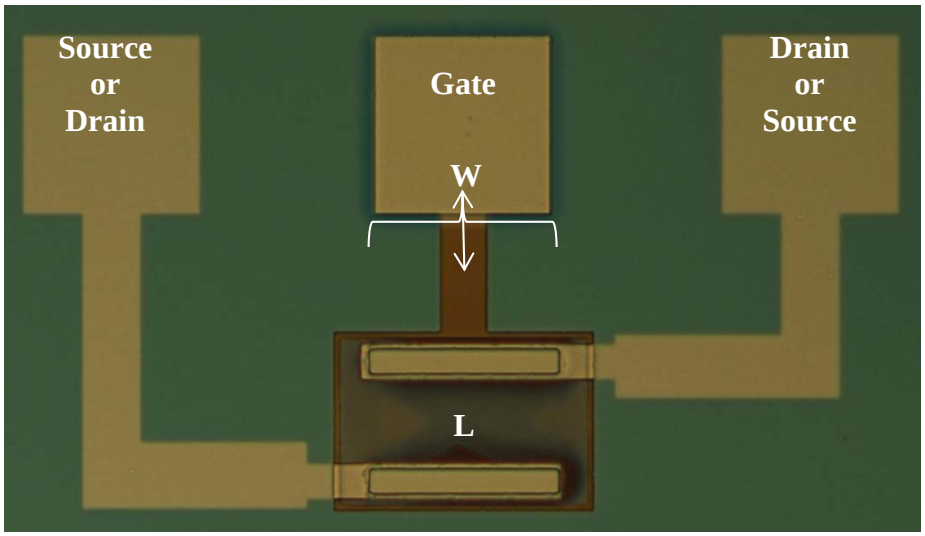

Fig. 1. Top view by optical microscopy from the TFT of ZnTe p-type built by photolithography.

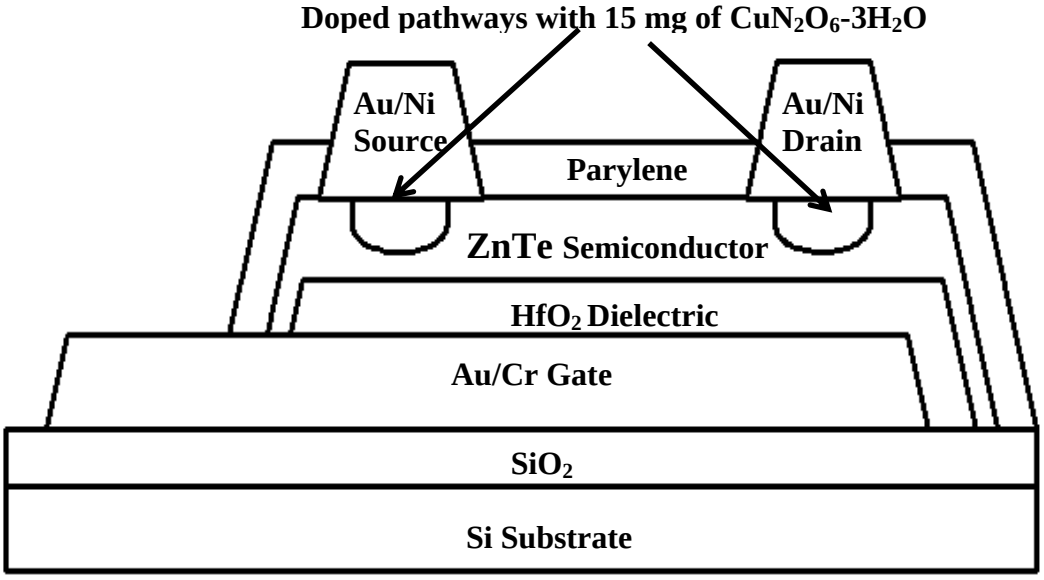

Fig. 2. Transversal section from the TFT of ZnTe p-type with doped pathways

3. Results and discussion

The figure 3 shows the curves (I_D-V_D) at different gate voltage V_G from the p-type ZnTe TFT with doped pathways at 15 mg of CuN_2O_6-$3H_2O$. We can see that the TFT are switching at these conditions. The specific contact resistance, ρ_c = 2.1 x 10^{-4} Ωcm^2 was measured by CLTM method. Additionally, a mobility of ~5 cm^2/Vs and carrier concentration of ~ 10^{17} cm^{-3} were obtained by Hall effect. A low contact specific resistance is necessary to have an ohmic contact between the metal and the semiconductor [11]. We applied V_G from +5 to -10 V with steps of 2.5 V to see the behavior of family curves (I_D-V_D). For all the TFTs, the gate currents I_G measured were around ~ 10^{-11} A, these leakage current are low compared with I_D that increased from ~10^{-8} to ~10^{-7} A in all the V_D range (0 to -10 V).

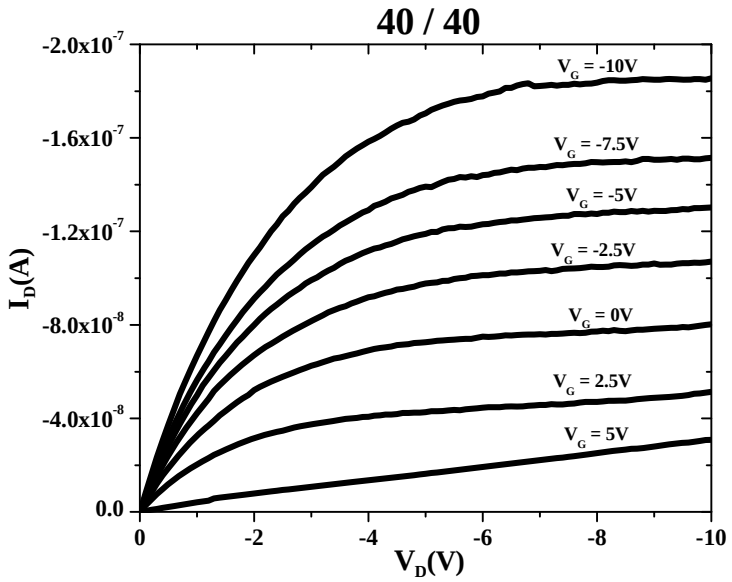

Fig. 3. I_D-V_D curves for TFTs with W/L = 40/40.

We could observe at $I_D = 7 \times 10^{-8}$ A at $V_D = 10$ V (p-channel on) at $V_G = 0$ V, instead of $I_D \sim 0$ A (p-channel off). This is related with the conductivity of the ZnTe layer. When we applied negative V_G from 0 to -10 V an active p-channel was formed at the interface ZnTe/SiO_2 and with the potential different between contacts source-drain the I_D across the channel started increasing, in this manner the TFT behaves in enhancement mode. You can see that any L, I_D increases with drain voltage V_D linearly, behaving like a resistor, depending on the model of the FET [12]. Shows that the curves (I_D-V_D) are saturated, however, not completely saturate because the conductive channel is ZnTe. However, when applying positive V_G 0 to +5 V decreased the I_D 2 times the I_D obtained at $V_G = 0$ V. We obtained values of first approximation of the mobility, μ (1×10^{-2} cm^2/Vs) and threshold voltage, V_{th} (~ 10 V) for W/L = 40/40 using the saturation regime ($\sqrt{I_D}$ vs V_G) [13]. This mobility is low for practical use, especially compared with the mobility of a-Si TFT equal to 1 cm^2 / Vs.

4. Conclusion

We could see that the thin-film transistor with 75 nm of ZnTe with doped pathways at 15 CuN_2O_6-$3H_2O$ and heated at 300 °C for 10 minutes was switching. However, the mobility is low for practical use.

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