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FABRICATION AND CHARACTERIZATION OF Al/n-CdSe SCHOTTKY BARRIER UNDER DIFFERENT ANNEALING TEMPERATURES

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A simple chemical reduction route has been followed to grow CdSe nanoparticles (size controlled) at room temperature. The grown sample is dispersed in ethanol. The dispersed samples are characterized structurally and optically. The result supports the formation of nanoparticles and hence an increase in band gap (E_g) compared to that of the bulk CdSe (E_g of the order of 1.74 eV). Capacitance-voltage and current-voltage measurements are performed on grown Schottky barrier Al/n-CdSe. The barrier height, ionized trap like-donors concentration, series resistance and diode ideality factor are measured for the samples grown under different annealing temperatures.

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Keywords: Quantum dots, Size effect, I-V and C-V characteristics, Annealing temperature effect, Ideality factor, Schottky diode

1. Introduction

Chalcogenides, especially of cadmium, lead and zinc, have proved their potential as efficient absorbers of electromagnetic radiation [1–6]. CdSe thin films are well known for their extensive applications as an optoelectronic material in solar cells [1,2].Cadmium selenide is an ideal material to be used as the window layer of heterojunction solar cells [3,4]. There are various methods [7-14] to prepare CdSe nanoparticles. Some of the above mentioned methods have certain drawbacks. These methods are not cost effective. Hence a simple chemical reduction route is preferred. It is well known that metal/semiconductor (MS) contacts are frequently used in integrated circuits, in light detectors and as solar cells. Schottky barrier diodes (SBDs) such as Al/CdSe, which has a rectifying nature, are among the simplest MS contact devices [15,16]. The existence of native oxide layers between metal and semiconductor influence the interface states and can modify the electrical properties of metal–semiconductor structures [17-20].

2. Experimental

A stoichiometric amount of anhydrous $CdCl_2$, selenium powder and sodium borohydride are taken. Ethylenediamine is used as a capping agent. Sodium borohydride on the other hand is used to initiate the reaction at room temperature. The stirring is continued for 3 hours at a particular speed. The grown samples are filtered and finally centrifuged.TEM, TED of the samples are taken using JEOL-JEM-200 transmission electron microscope operating at 200 kV. Optical absorption measurements of the dispersed samples are studied in the range of 500-800 nm using Shimadzu Pharmaspec 1700 UV-VIS spectrometer. Photoluminescence spectra of the same sample is obtained using Hitachi F-7000 FL Spectrophotometer.

Thin film of the CdSe nanoparticles is grown from the dispersed sample. The pre-cleaned glass substrate is dipped in to the dispersed solution for at least for 6 hrs. Uniformly thin film of CdSe nanoparticles get deposited on the glass substrate. The film is annealed at different

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temperatures in the range 333–363K. Al is deposited on CdSe thin film by vacuum evaporation for Schottky contact. Capacitance-voltage measurements are performed on Al/n-CdSe devices using a computerized controlled 410 CV meter with an operating frequency at 1MHz. The measurement of the I-V characteristics are taken using an electrometer (Kiethly 6514).

3. Result and discussion

3.1 Structural Properties

TEM image of the bright field of CdSe nanoparticles and its selected area (electron) diffraction (SAED) pattern are shown in figure 1(a) and 1(b) respectively. Crystal size is determined to be approximately 5–8 nm. A clear hexagonal phase of the as-prepared CdSe nanoparticles is revealed in the TED pattern figure 1(b). From Hot Probe measurement of the thin film of CdSe, the type of the sample is detected and is found to be n-type.

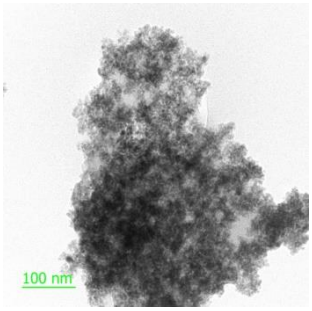

Fig. 1(a) The TEM image of as prepared CdSe nanoparticles

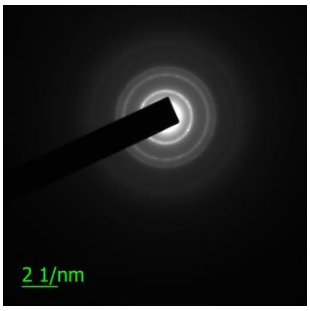

Fig. 1(b) The SAED pattern of CdSe nanoparticles in Fig. 1(a)

3.2 Optical Properties

Fig. 2 displays the variation of optical absorbance with wavelength of the as-prepared nanoparticles. Optical absorption coefficient has been calculated in the wavelength region of 500 – 800 nm. The band gap of the as- prepared nanoparticles is determined from the relation [21].

$$(\alpha h\nu) = C\,(h\nu - \Delta E_g)^{1/2} \qquad (1)$$

where C is a constant, ΔE_g = 2.02 eV and is shown in the inset of figure (2), whereas the bulk band gap is 1.74 eV. It confirms that the absorption peak is shifted from their bulk edge 704 nm. This is due to the quantum confinement effect.

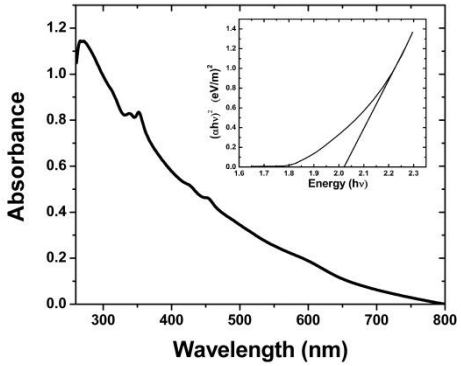

Fig. 2. displays the variation of optical absorbance with wavelength and as well the determination of band gap of as prepared CdSe nanoparticles in its inset

Fig. 3 shows the photoluminescence spectrum of CdSe nanoparticles. The photoluminescence spectrum of the as-prepared CdSe nanoparticles shows a sharp peak at 615 nm and correspond to band edge luminition [8-12].

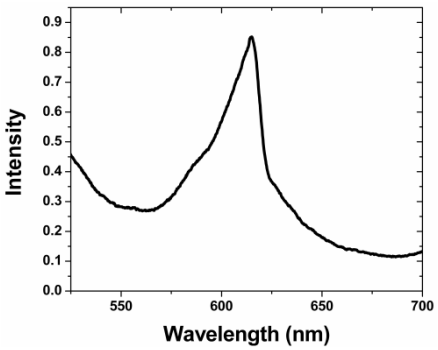

Fig. 3. displays the photoluminescence spectrum of the as-prepared CdSe nanoparticles

3.3 Capacitance-Voltage Measurement

Capacitance voltage dependence is studied for samples annealed at different temperatures under reverse biasing voltages at 1MHz. and is shown in Figure 4(a). Figure 4(b) indicates that the capacitance is bias independent at strong reverse bias $(V \leq -6.4V)$, which corresponds that the sample is fully depleted. A locally linear behavior is also noted therein as the bias increases in all annealed temperatures. The depletion layer capacitance is defined as

$$C = \frac{dQc}{dV} \tag{2}$$

where dQc is the incremental increase in charge with the incremental change of applied voltage dV.

The linear portion of the curve is extrapolated in Figure 4(b) to voltage axis. From the intercept the barrier potential (V_b) is found for each annealed condition. Thus the barrier height Φ_b is found out.

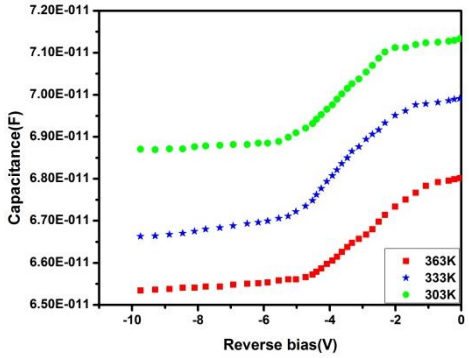

Fig. 4(a). The capacitance-voltage dependence in reverse biasing of Al/n-CdSe thin film at different annealed temperatures

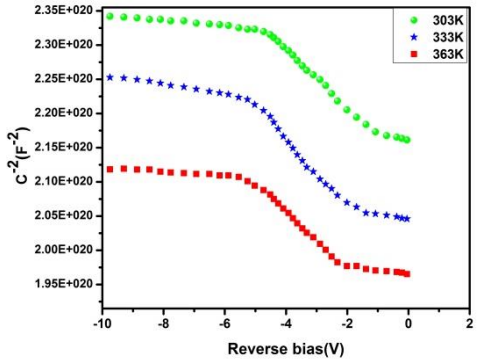

Fig. 4(b). The $1/C^2$ - V dependence in reverse biasing of Al/n-CdSe thin film at different annealed temperatures

The capacitance per unit area for one-sided abrupt junction at equilibrium is given by [17]

$$C=\frac{dQc}{dV}=\frac{d(qN_dW)}{d[q(N_d/(2\varepsilon\varepsilon_0))W^2]}=\frac{\varepsilon\varepsilon_0}{W}, \tag{3}$$

where

$$W=\sqrt{\frac{2\varepsilon\varepsilon_0 V_b}{qN_d}}, \tag{4}$$

where N_d denotes the ionized traps like donor, V_b is the built-in potential, q is the electronic charge and ε_0 is the free space permittivity, W is the width of the depletion region and ε the relative permittivity of the CdSe thin films.

Now for the reverse bias condition,

$$W=\sqrt{\frac{2\varepsilon\varepsilon_0(V_b+V)}{qN_d}} \tag{5}$$

Thus the depletion layer capacitance can be expressed as

$$C^{-2}=\frac{2(V_b+V)}{q\varepsilon\varepsilon_0 A^2 N_d} \tag{6}$$

where A is the area of the device. The ionized trap N_d is obtained from the slope of $1/C^2$ versus V relationship. From the extrapolation intercept of $1/C^2$ with the abscissa, V_b is obtained. The values of N_d and V_b obtained at different annealed temperatures are shown in Table 1.The potential across the depletion region equals the built-in potential V_b in the semiconductor devices in thermal equilibrium.

Table 1. Parameters calculated from CV and IV measurements at different annealed temperatures.

Parameters calculated from CV Measurement				Parameters calculated from IV measurement	
T(K)	V_b(V)	N_d(cm^{-3})	Φ_b(eV)	R_s(KΩ)	η
303	0.588	$5.6X10^{16}$	1.03	11.869	1.53
333	0.307	$5.7X10^{16}$	0.79	10.616	2.08
363	0.103	$6.09X10^{16}$	0.63	8.479	2.23

From CV measurements the value of barrier height Φ_b can be calculated by the following well-known equation,

$$\Phi_b = V_b + V_p \tag{8}$$

where V_p is the potential difference between the Fermi level and the top of the conduction band in CdSe . Knowing the concentration N_d, V_p can be calculated using the following relation,

$$V_p = kT \ln\left(\frac{N_c}{N_d}\right) \tag{9}$$

where $N_c = 1.8 \times 10^{24}\ cm^{-3}$ is the density of states in the conduction band for CdSe. The Φ_b values for the Al/n-CdSe device annealed at different temperatures are shown in Table-1.

Fig. (5) shows the variation of the capacitance versus forward bias voltage of the sample annealed at different temperatures. The barrier height Φ_b decreases with increase of annealing temperature (Table 1). This is possibly due to the thermal generation of carriers on the semiconductor side. The thermally generated carriers increase with an increase of annealing temperature. These carriers neutralize the immobile charges on the semiconductor side. Thus the barrier height reduces with annealing temperature.

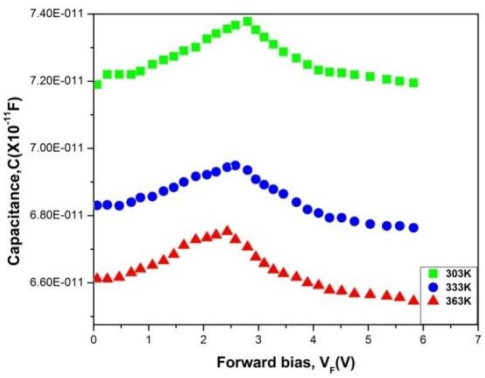

Fig.5. The variation of the capacitance in the forward biasing for samples annealed at different temperatures

The capacitance in the forward bias corresponds to diffusion capacitance which is due to diffusion of mobile charges. Diffusion capacitance decreases with increase of annealing

temperature, this is possibly due to decrease of concentration of mobile charges with annealing temperature.

3.4 Current–Voltage characteristics

The I-V Characteristics of Al/n-CdSe device under forward and reverse biasing condition at different annealed temperature are shown in Figure 6. The curves shown in the figure are very much similar to that of a metal/semiconductor (MS) Schottky barrier.

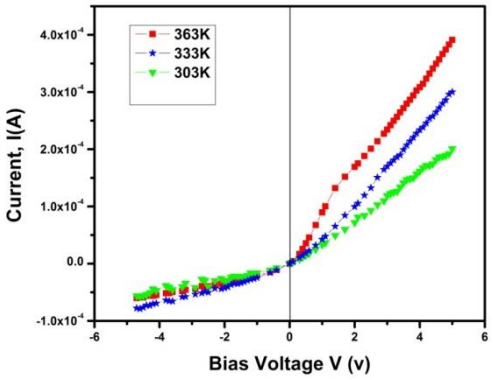

Fig.6 I-V characteristics of the Al/n-CdSe device in forward and reverse biasing condition

The asymmetrical I-V characteristics under the forward and reverse biasing voltages are observed. The I-V plot indicates that barrier potential is low for highest annealed temperature sample as confirmed by C-V measurement.

The current as a function of applied biasing voltages is given by [22]

$$I = I_S\left[\exp\left(\frac{q(V-IR_S)}{\eta kT}\right) - 1\right] \tag{10}$$

$$\frac{dV}{d(\ln I)} = IR_S + \frac{\eta kt}{q} \tag{11}$$

The series resistance(R_s) is calculated from the slope of the linear plot shown in Figure 7,while ideality factor (η) is determined using Eq. (11) from the y-axis intercept of the linear fit. The η and R_s at different annealed temperatures are listed in Table 1.

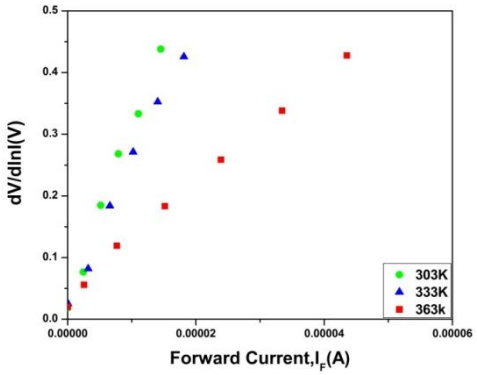

Fig. 7. dV/d(lnI) versus I for Al/n-CdSe thin film annealed at different temperature

4. Conclusions

Deposition of semiconductor on a metal surface leaves a interfacial layers at the junction. And the semiconductor surface contains surface states due to incomplete covalent bonds. Thus it can lead to changes in the values predicted on the work function of two isolated materials.

Potential drop in the interfacial layer and presence of excess current and the recombination current through the interfacial states between the semiconductor/insulator layers is the probable reason to get the high value of η. Significant variation is observed in all parameters as the annealed temperature is increased to 363K. Thus with annealing there is a large shift from the ideality condition for such metal-semiconductor junction

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