

## Modified nonlinear ion drift model for TiO<sub>2</sub> memristor: a temperature dependent study

S. Panda<sup>a</sup>, C. S. Dash<sup>a,\*</sup>, R. Jothiramalingam<sup>b</sup>, H. Al-Lohedan<sup>b</sup>

<sup>a</sup>*Department of Electronics and Communication Engineering, Centurion University of Technology and Management, Odisha, Bhubaneswar, 752050, India*

<sup>b</sup>*Department of Chemistry, College of Science, King Saud University, P.O.Box 2455, Riyadh 11451, Saudi Arabia*

The creation and optimisation of memristor models with different topologies and physical mechanisms have received increasing attention in recent years. Memristors, known for their unique resistive switching mechanism, have garnered significant interest as promising components for next-generation computing. However, to effectively design and test memristor-based circuits, it is crucial to have a mathematical representation of the experimentally determined current-voltage characteristics of memristors. This paper proposes a model and conducts an analysis that offers insights into memristor technology, beginning with its characteristics and extending to simulations involving various parameters. The proposed model and its dependency on temperature are implemented using MATLAB. The model captures changes in current characteristics concerning the fundamental voltage without using any window functions. Thus, it accurately represents the variation in memristance with temperature, contributing to a more precise and observed modelling approach.

(Received March 22, 2024; Accepted May 24, 2024)

*Keywords:* Memristor, Titania, Resistive switching, Ion migration, Filamentary conduction

### 1. Introduction

Resistive random-access memory (ReRAM) technology [1] is highly promising because of its simple structure, low power consumption, and high switching speed [2], making it suitable for memory applications [3]. It consists of a thin metal oxide film sandwiched between the top and bottom electrodes [4]. Memristor-based memory [5], often considered a type of emerging ReRAM [6], offers unique properties, such as high density, ultra-low power consumption, excellent scalability, nonvolatility [7], and suitability for neuromorphic computing [8]. The concept of the memristor was first demonstrated by Strukov et al. They achieved this by sandwiching TiO<sub>2</sub> layers between platinum (Pt) electrodes, resulting in pinched hysteresis loops and resistive switching characteristics [7], [9]. This led to the classification of memristors as ReRAM. Furthermore, memristors have been widely used in various applications, such as chaotic circuits [10], oscillators, filters, programmable analog circuits, sensors, cellular neural networks [11], fuzzy processors [11], and nonvolatile memory devices [7].

For effective circuit implementation, it is crucial to use memristor models [12, 13]. Numerous models have been proposed to simulate the behaviour of practical memristor devices, and filamentary conduction is widely recognized as the mechanism responsible for resistive switching (RS) [7], [14,15]. During the process of filamentary conduction, the application of a positive bias voltage between the top and bottom Pt electrodes leads to the formation of a filament within the TiO<sub>2</sub> RS layer [16], transforming the device into a low resistance state (LRS) [17]. However, when the applied bias is reversed, the filament ruptures, causing the device to enter a high resistance state (HRS) [18]. Given the nanoscale dimensions of the memristor, the phenomenon of filamentary conduction might be dependent on temperature. Although many

---

\* Corresponding author: [chandu0071@gmail.com](mailto:chandu0071@gmail.com)  
<https://doi.org/10.15251/JOR.2024.203.345>

memristor models exist, such as the linear ion drift memristor model [19], nonlinear ion drift memristor model [20], Simmon tunnel barrier model [21], threshold adaptive model [13],[22], and voltage threshold adaptive model, [13],[22], none of them consider the effect of temperature when describing the RS phenomena of memristors [7],[23]. Some recent studies have reported the effect of temperature [24],[25], but none of them have definitively explained the phenomenon of filamentary conduction [7],[26]. In this study, we introduced a dynamic mechanism [27] to determine the RS characteristics of TiO<sub>2</sub>-based memristors, considering the impact of temperature on charge carrier mobility [28]. This mechanism was used to modify the model to incorporate the nonlinearity of ion dynamics and the temperature-dependent nature of ion migration.

The remainder of this paper is organized as follows. In Section 2, we present the proposed model, explaining the mechanism behind filament formation due to ion drift and discussing the associated V-I characteristics. In Section 3, we address the effect of temperature on Z<sub>on</sub> and Z<sub>off</sub> variations. Further, in this section, we investigate the effect of temperature on memristance, total charge, and diffusion coefficient. In Section 4, we present concluding remarks and outline potential directions for future research.

## 2. Experimental

### 2.1. Proposed model

In this section, a model based on which the calculations of various characteristics of memristor are to be studied and a simulation for an experimental model on V-I characteristics is to be performed. The proposed model, here, in fact, is based on the mechanism of ion transport as was discussed by Mazady and Anwar [29]. They have considered the observations on V-I characteristics of Pt/TiO<sub>2</sub>/Pt memristor as addressed by Yang et al. [30]. Here the filament-assisted current as shown in Fig.1 dependent on the redox chemistry at the contacts and flows from the tip of the growing filament to the opposite contact.

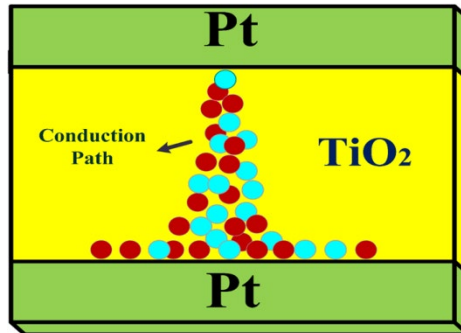


Fig. 1. Filament-assisted current in the Pt/TiO<sub>2</sub>/Pt memristor from the tip of the growing filament to the opposite contact.

The reduction mechanism is described as follows:

With a positive bias voltage at anode, the reduction of Ti<sup>+4</sup> (TiO<sub>2</sub>) into Ti<sup>+3</sup> (Ti<sub>4</sub>O<sub>5</sub><sup>+2</sup>) occurs at the anode [7], [29, 30] and further followed by



The drifted positive ions Ti<sub>4</sub>O<sub>5</sub><sup>+2</sup> moves towards the cathode and their interaction with O<sub>2</sub><sup>-</sup> ions produce Ti<sub>2</sub>O<sub>3</sub> as given by the reaction



However, accumulation at cathode of  $2\text{Ti}_2\text{O}_3$ , a metastable stage of  $\text{TiO}_2$ , gives rise to the high conductivity filaments due to its growth towards the anode. According to classical microscopic approach, the ionic transport in solids is a hopping mechanism [27], [31]. As the temperature rises, the mechanism of conduction of transition metal ions changes in semiconductor metal oxides. The variable range hopping (VRH) [7],[30],[32] which is a process of switching between states that are located near to the Fermi level in finite localized states [33].

In low temperatures ( $T < 300$  K), VRH is driven by ES (EfrosShklovskii) [34] hopping and in high temperatures ( $T > 300$  K), VRH is driven by Mott's Law [24], [35]. The conductivity of  $\text{TiO}_2$  related to the above discussion can be expressed as:

$$\sigma = \sigma_{0,\text{Mott}} T^{-2s} \exp \left[ - \left( \frac{T_{0,\text{Mott}}}{T} \right)^s \right] + \sigma_{0,\text{ES}} T^{-2s} \exp \left[ - \left( \frac{T_{0,\text{ES}}}{T} \right)^s \right] \quad (3)$$

Basically,  $T_0$  is the characteristic temperature coefficient that depends upon the density of state in the Fermi level, 's' is a constant that depends on the type of hopping process, and  $\sigma_0$  is a pre-exponential factor that depends on hopping [19],[24],[36]. In Mott's law,  $\sigma_{0,\text{Mott}}$  represents the pre-exponential factor and in ES law,  $\sigma_{0,\text{ES}}$  represents the pre-exponential factor [24], [37].

## 2.2. Dependence of mobility on temperature

Using one dimensional potential barrier a temperature dependent equation of mobility can be considered and with the help of conductivity, it can be determined from the equation given below that the mobility in  $\text{TiO}_2$  memristors relative to the temperature

$$\mu_v = \frac{\sigma \cdot M(\text{TiO}_2)}{N \cdot e \cdot n \cdot \text{density}(\text{TiO}_2)} \quad (4)$$

Here  $\mu$  is the mobility,  $M(\text{TiO}_2)$  is the molecular weight of  $\text{TiO}_2$ ,  $N = 6.023 \times 10^{23}$  per mole is the Avogadro's number,  $e$  is the charge of electron,  $n$  is the number of electron in lattice fraction and density ( $\text{TiO}_2$ ) is taken as  $4.26 \times 10^9$ .

In the present model with the charge carrier mobility equation (4), we can describe the dependence of mobility on temperature [13], [19], [38]. This model considers two resistors in series: one representing the high concentration of the dopant region (high conductance) [7], [13], [24], [39] and the other representing the oxide region (low conductance) [7], [13], [24], [30]. Mobility derived at higher temperatures exhibits a more linear variation than the reported mobility, which ranges from 300 K to 800 K. After examining this model, the performance of mobility at different temperatures is shown in Fig.2.

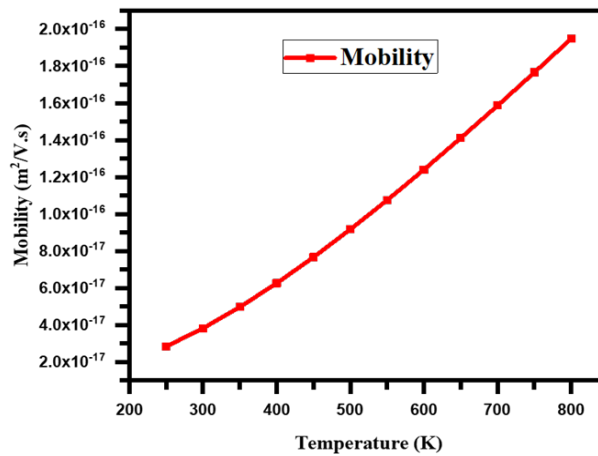


Fig. 2. Temperature dependent mobility of the proposed model.

### 2.3. Resistances ( $Z_{on}$ and $Z_{off}$ )

Resistances ( $Z_{on}$  and  $Z_{off}$ ) are present in series with each other, as shown in Fig. 3, where one of these resistances represent  $TiO_2$ , whereas the other represents  $TiO_{2-x}$  [40]. The former is stoichiometric, whereas the latter contains oxygen vacancies. The undoped  $TiO_2$  region of length  $l_{ud}$  with very low oxygen deficiency is denoted as state  $Z_{on}$  [41, 42], whereas the doped  $TiO_{2-x}$  region of length  $l_d$  is denoted as  $Z_{off}$  [41, 42]. They can be explicitly expressed as

$$Z_{on} = \frac{l_d}{A \cdot \sigma} \quad (5)$$

$$Z_{off} = \frac{l_{ud}}{A \cdot \sigma} \quad (6)$$

where  $A$  is the area of the memristor device. The memristor exhibits a nonlinear relationship between the magnetic flux linkage  $\phi_m(t)$  and the amount of electric charge  $q(t)$ , which has passed through it is given by

$$f(\phi_m(t), q(t)) = 0 \quad (7)$$

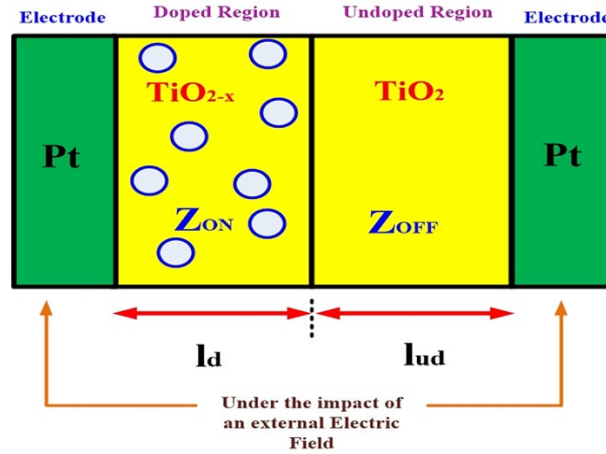


Fig. 3. Doped and undoped regions in a memristor.

### 2.4. The associated V-I characteristics

The concept of  $\phi_m(t)$ , derived from the circuit properties of an inductor in a generalised manner, can be interpreted as the temporal integration of voltage. Its relationship with  $q$  depends on their values as well as the derivative of one with respect to the other. The memristance function  $m(q)$  defines the flux change with charge, and it is dependent on charge [43] as follows:

$$m(q) = \frac{d\phi_m}{dq} \quad (8)$$

$$m(q(t)) = \frac{d\phi/dt}{dq/dt} = \frac{V(t)}{I(t)} \quad (9)$$

Here, Ohm's law follows if  $m(q(t))$  remains constant and  $m(q(t))$  being nontrivial, has a twist resulting in to non-equivalence of equations (8) and (9) [44]. As both  $q(t)$  and  $m(q(t))$  have power to change over the time, the time dependent voltage can be represented as

$$V(t) = I(t) \cdot m(q(t)) \quad (10)$$

This establishes a direct relationship between voltage and current as long as memristance remains constant with charge [45]. However, for a non-zero current, the time-dependent charge comes into play and the voltage versus current relationship is determined through the model expression that relates current to voltage, expressed as follows:

$$I(i) = k1 \times ((W(i)^n \times \beta \times \sinh(\alpha \times V(i)) + \frac{c \times V(i) \times (\exp((- \mu \times \gamma) / (T \times Q \times x)) - 1) \times T}{(Z_{on} / Z_{off})}) \quad (11)$$

where  $I$  represents the current,  $\mu$  = mobility,  $c$ ,  $\alpha$ ,  $\beta$ ,  $\gamma$  and  $k1$  are fitting parameters,  $T$  is the temperature in Kelvin,  $x$  is distance between the Pt electrodes,  $Z_{off}$  and  $Z_{on}$  are OFF and ON state resistances respectively and  $Q$  is the charge of ion.

When calculations are performed at different temperatures using equation (11), it yields different current values for each temperature, as shown in Fig. 4(a). The same data is plotted for the minimum and maximum temperatures of 300 K and 700 K, respectively, in Fig. 4(b). The temperature dependence of memristors is not precisely known. In the present model, the temperature dependent exponential factor is considered as a preliminary attempt to understand it. The obtained nonlinear Voltage and Current relationship are found to produce hysteresis loop, where the pinched hysteresis loop is input voltage and temperature dependent [46, 47].

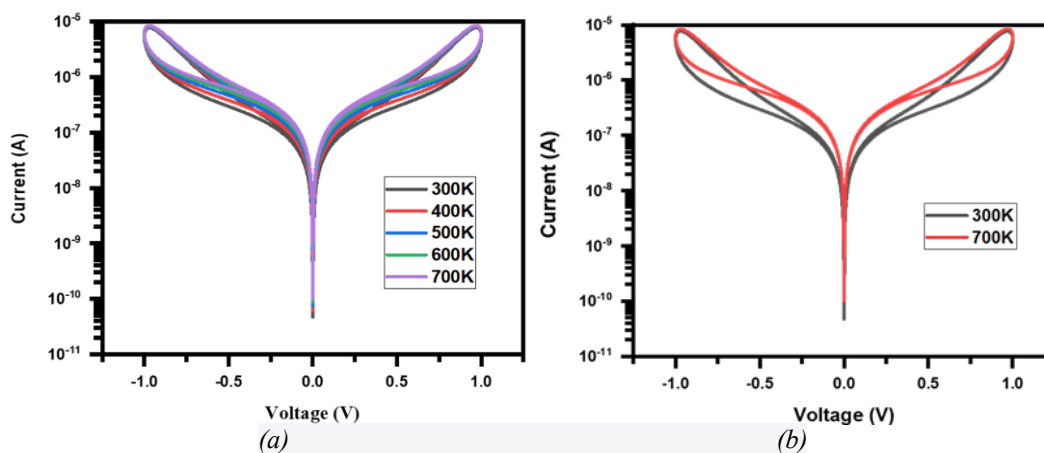


Fig. 4 (a). The effect of temperature on the current based on the proposed memristor model at 300K, 400K, 500K, 600K and 700K and Fig.4(b). Comparison between the V-I curves taken between Minimum Observed Temperature 300K and Maximum Observed Temperature 700K.

The hysteresis loop area is seen to decrease with increase in temperature as shown in Fig.4(a) and Fig.4(b), thus explaining the higher memory capacity of this technology [48-49]. Further, its higher memory density also produces faster access [48]. It is also found that the ratio between  $Z_{off}$  and  $Z_{on}$  (two variable resistances which will be explicitly discussed in the Section 3) of the memristor, i.e.,  $\frac{Z_{off}}{Z_{on}}$  is hysteresis loop area itself [48] and thus it is temperature dependent. In this regard the observations have been taken at temperatures 300K to 700K in the interval of 100K to prove the  $\frac{Z_{off}}{Z_{on}}$  dependency on temperature as it has been found in the Fig.4(a) and Fig.4(b) where it is seen that there is a decrease in  $\frac{Z_{off}}{Z_{on}}$  with rise in temperature [48-52]. We next go over to section 3, where it will be discussed about the effect of temperature on  $Z_{on}$  and  $Z_{off}$ .

### 3. Results and discussion

#### 3.1. The effect of temperature on $Z_{on}$ and $Z_{off}$

Temperature-dependent simulated results of  $Z_{on}$  and  $Z_{off}$  are presented in Fig. 5(a) and Fig. 5(b), respectively. When the frequency is constant, temperatures vary from 200 K to 800 K. These simulations provide insight into how resistance values change with temperature.

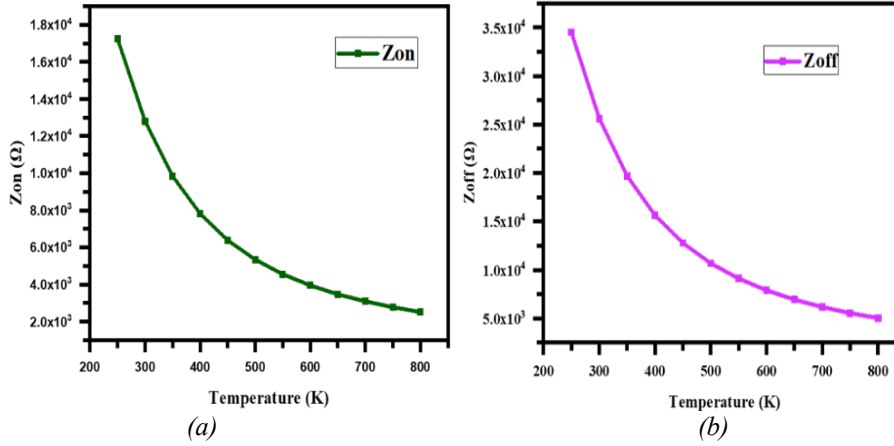


Fig. 5. (a) The variation of  $Z_{on}$  resistance with rise in temperature and Fig. 5.(b) The variation of  $Z_{off}$  resistance with rise in temperature.

The ON state region with low  $Z_{on}$  exhibits very high conductivity, whereas the OFF-state region with high  $Z_{off}$  behaves in the opposite manner, displaying much lower conductivity [53]. As depicted in Fig. 6, the LRS and HRS are closely related to the performance of  $Z_{on}$  and  $Z_{off}$  [54], affirming that filamentary conduction effectively delivers the expected outcomes.

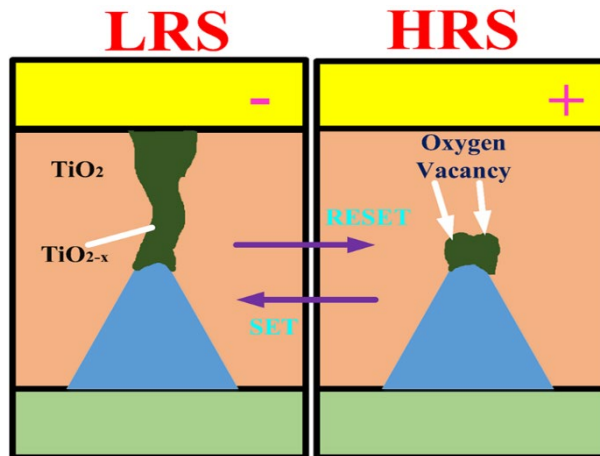


Fig. 6. LRS and HRS relationship to the performance of  $Z_{on}$  and  $Z_{off}$  silver modified Rutile  $TiO_2$ .

As shown in Fig. 5(a) and Fig.5(b), as temperature increases while keeping amplitude and frequency constant, both  $Z_{on}$  and  $Z_{off}$  resistances decrease. This finding indicates that the sensitivity of electrical conductivity to changes in temperature [55]. In the next section, we discuss the effect of temperature on memristance, total charge and diffusion coefficient .

### 3.2. Effect of temperature on memristance, total charge and diffusion coefficient

In the proposed model, as depicted in Fig. 7, in the temperature range of 250 K to 700 K, memristance rises with increase in temperature [23, 24], [56]. Although there is a minor uptick in memristance at higher temperature variations, the HRS/LRS ratio remains relatively stable because both HRS and LRS decrease with temperature at nearly equal rates.

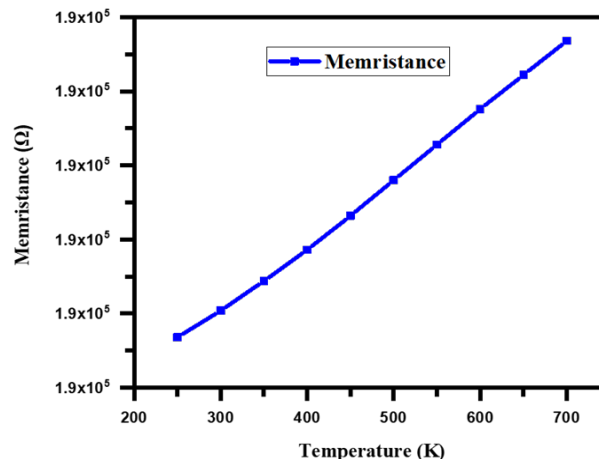


Fig. 7. Memristance variation with temperature.

However, very high temperatures may lead to information loss due to inner diffusion within the memristor. These findings demonstrate a significant increase in ON current and rapid resistance switching in the memristor at higher temperature ranges. Temperature affects not only the diffusion rate but also the lowest and highest attainable resistances [24], [56]. The calculated values of mobility,  $Z_{on}$ ,  $Z_{off}$  and memristance, which are presented in Table 1, exhibit variations with temperature, and they align with expected behavioural patterns.

Table 1. The performance of the model at different temperatures.

Temperature (K)	Mobility ( $m^2/V.s$ )	$Z_{on}$ ( $\Omega$ )	$Z_{off}$ ( $\Omega$ )	Memristance ( $\Omega$ )
200	$2.045 \times 10^{-17}$	$2.394 \times 10^4$	$4.788 \times 10^4$	$1.911 \times 10^5$
300	$3.824 \times 10^{-17}$	$1.28 \times 10^4$	$2.56 \times 10^4$	$1.915 \times 10^5$
400	$6.263 \times 10^{-17}$	$7.817 \times 10^3$	$1.563 \times 10^4$	$1.919 \times 10^5$
500	$9.169 \times 10^{-17}$	$5.339 \times 10^3$	$1.067 \times 10^4$	$1.924 \times 10^5$
600	$1.2403 \times 10^{-16}$	$3.947 \times 10^3$	$7.895 \times 10^3$	$1.928 \times 10^5$

A comparative analysis of memristance performance in relation to charge carrier mobility at various temperatures (200K to 700K) is presented in Fig.8(a). Additionally, the temperature dependence of the maximum charge that the memristor was able to memorise is shown in Fig.8(b). It is evident that when temperature rises, less charge is allowed to flow through the memristor. The reason for this is because when temperatures rise, significant rise in oxygen vacancies occur, which causes charge carriers to scatter. Further, Fig.8(c) depicts the linear relationship between temperature and diffusion coefficient.

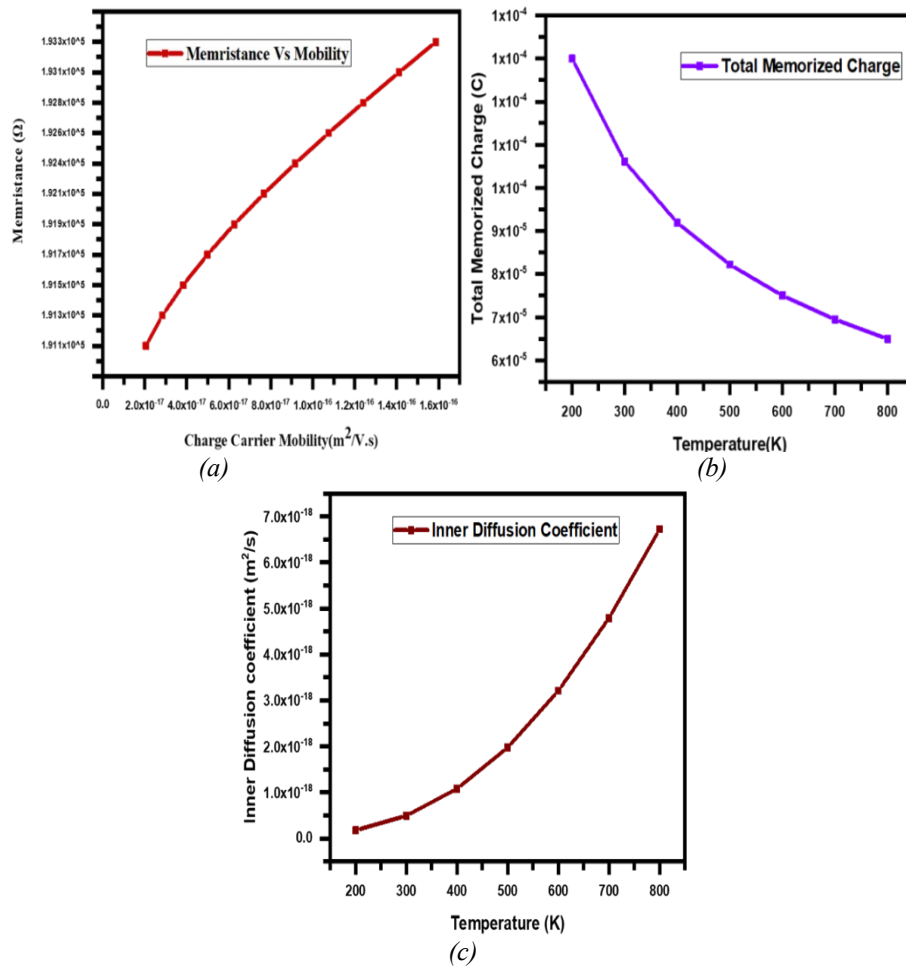


Fig. 8. (a) Performance of memristor concerning charge carrier mobility plotted at different temperatures 200K to 700K, Fig.8 (b) Influence of temperature on the charge capacity and Fig.8(c) Variation of the inner diffusion coefficient of memristor with temperature.

#### 4. Conclusion

This study investigated the effect of temperature on various memristor parameters, including mobility,  $Z_{on}$ , and  $Z_{off}$ , along with V-I characteristics and hysteresis loops. The calculated  $Z_{on}$  and  $Z_{off}$  decrease with temperature, affecting the switching and V-I characteristics. The graphical representations of these characteristics reveal hysteresis loops, the area of which decreases with increasing temperature. This reduction in loop area suggests a decrease in memory performance as temperature increases. Furthermore, memristances were calculated and plotted, which increased with a rise in temperature from 250 K to 700 K. All simulations were based on MATLAB Simulink. From these findings, we can conclude that memristors, owing to their compact dimensions and high conductivity, hold promise for future applications in neural networks and signal processing. These findings provide valuable insights for potential future work in these areas.

#### Acknowledgments

The authors extend their appreciation for funding to Researchers Supporting Project number (RSP2024R354), King Saud University, Riyadh, Saudi Arabia



## References

- [1] Y.Chen, IEEE Transactions on Electron Devices, 67(4), 1420-1433 (2020); <https://doi.org/10.1109/TED.2019.2961505>
- [2] M.Nakayama, 2017 IEEE International Memory Workshop (IMW), 1-4 (2017); <https://doi.org/10.1109/IMW.2017.7939099>
- [3] M.Uek., K.Takeuchi, T.Yamamoto, A.Tanabe, N.Ikarashi, M.Saitoh., T.Nagumo, Sunamura, H., Narihiro, M., Uejima, K. and Masuzaki, K., IEEE, T108-T109 (2015); <https://doi.org/10.1109/VLSIT.2015.7223640>
- [4] Liu, S.H., Yang, W.L., Wu, C.C., Chao, T.S., Ye, M.R., Su, Y.Y., Wang, P.Y. Tsai, IEEE Electron Device Letters, 34(1), 123-125(2012); <https://doi.org/10.1109/LED.2012.2224633>
- [5] Workshop S. Hamdioui, H. Aziza and G. C. Sirakoulis, 2014 9th IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS), Santorini, Greece, 1-7 (2014); <https://doi.org/10.1109/DTIS.2014.6850647>
- [6] E.Gale, Semiconductor Science and Technology, 29(10), 104004(2014); <https://doi.org/10.1088/0268-1242/29/10/104004>
- [7] C.S.Dash, S.Sahoo, S.R.S.Prabaharan, Solid State Ionics, 324(2018); <https://doi.org/10.1016/j.ssi.2018.07.012>
- [8] Y.Li, Z.Wang, R.Midya, Q.Xia, J.J.Yang, Journal of Physics D: Applied Physics, 51(50), 503002 (2018); <https://doi.org/10.1088/1361-6463/aade3f>
- [9] Y.H.Ting, J.Y.Chen, C.W.Huang, T.K.Huang, C.Y. Hsieh, W.W.Wu, Small, 14(6), 1703153 (2018); <https://doi.org/10.1002/sml.201703153>
- [10] J.R.Piper, J.C.Sprott, IEEE Transactions on Circuits and Systems II: Express Briefs, 57(9), 730-734 (2010); <https://doi.org/10.1109/TCSII.2010.2058493>
- [11] P.Mani, R.Rajan, L.Shanmugam, Y.H.Joo, Information Sciences, 491(2019); <https://doi.org/10.1016/j.ins.2019.04.007>
- [12] L.Chua, Handbook of memristor networks (2019); <https://doi.org/10.1007/978-3-319-76375-0>
- [13] S.Kvatinsky, E.G.Friedman, A. Kolodny U.C Weiser, IEEE transactions on circuits and systems I: regular papers, 60(1), 211-221 (2012); <https://doi.org/10.1109/TCSI.2012.2215714>
- [14] V.A. Demin, A.I.Ilyasov, V.V.Rylkov, P.K.Kashkarov, M.V.Kovalchuk, Nanobiotechnology Reports, 18(2), 305 (2023); <https://doi.org/10.1134/S2635167623700180>
- [15] H.Wang, L.Hu, W.Han, Journal of Alloys and Compounds, 854(2021); <https://doi.org/10.1016/j.jallcom.2020.157200>
- [16] L.Yang, Forschungszentrum Jülich 17 (2011).
- [17] B.J.Choi, S.Choi, K.M.Kim, Y.C.Shin, C.S.Hwang, S.Y.Hwang, S.S.Cho, S.Park, S.K.Hong, Applied physics letters, 89(1), (2006); <https://doi.org/10.1063/1.2219726>
- [18] Y.Yu, C.Wang, C.Jiang, I.Abrahams, Z.Du, Q.Zhang, J. Sun, X. Huang, Applied Surface Science, 485(2019); <https://doi.org/10.1016/j.apsusc.2019.04.119>
- [19] T.A. Anusudha, S.R.S.Prabaharan, AEU-International Journal of Electronics and Communications, 90(2018); <https://doi.org/10.1016/j.aeue.2018.04.020>
- [20] S.Thomas, S.Prakash, K.Priya, 2017 International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS) IEEE, 2189-2192(2017); <https://doi.org/10.1109/ICECDS.2017.8389839>
- [21] M.R.Rudra, R.J.Pieper, IETE Journal of Research, 61(4), 440-443(2015); <https://doi.org/10.1080/03772063.2015.1026851>
- [22] S.Kvatinsky, M.Ramadan, E.G.Friedman, A.Kolodny, IEEE Transactions on Circuits and Systems II: Express Briefs, 62(8), 786-790(2015); <https://doi.org/10.1109/TCSII.2015.2433536>
- [23] D.B.Strukov, H.Kohlstedt, MRS bulletin, 37(2), 108-114 (2012); <https://doi.org/10.1557/mrs.2012.2>
- [24] J.Singh, B.Raj, Engineering science and technology, an international journal, 21(5), 862-8 (2018); <https://doi.org/10.1016/j.jestch.2018.07.016>

- [25] R.S.Williams, M.D.Pickett, J.P.Strachan, 2013 IEEE International Symposium on Circuits and Systems (ISCAS) IEEE 93-104 (2013); <https://doi.org/10.1109/ISCAS.2013.6571821>
- [26] S.C.Tsai, H.Y.Lo, C.Y.Huang, M.C.Wu, Y.T.Tseng, F.C.Shen, A.Y.Ho, J.Y.Chen W.W.Wu, *Advanced Electronic Materials*, 7(10), 2100605 (2021); <https://doi.org/10.1002/aelm.202100605>
- [27] D.Ravaine, *Journal of Non-Crystalline Solids*, 73(1-3), 287-303(1985); [https://doi.org/10.1016/0022-3093\(85\)90355-2](https://doi.org/10.1016/0022-3093(85)90355-2)
- [28] D.Acharyya, A.Hazra, P.Bhattacharyya, *Microelectronics reliability*, 54(3), 541-560(2014); <https://doi.org/10.1016/j.microrel.2013.11.013>
- [29] A.Mazady, M.Anwar, *IEEE transactions on electron devices*, 61(4), 1054-1061 (2014); <https://doi.org/10.1109/TED.2014.2304436>
- [30] J.J.Yang, M.D.Pickett, X.Li, D.A.Ohlberg, D.R.Stewart, R.S.Williams, *Nature nanotechnology*, 3(7), (2008); <https://doi.org/10.1038/nnano.2008.160>
- [31] J.Lau, R.H.DeBlock, D.M.Butts, D.S.Ashby, C.S.Choi, B.S.Dunn, *Advanced Energy Materials*, 8(27), (2018); <https://doi.org/10.1002/aenm.201800933>
- [32] Y.L.Zhao, W.M.Lv, Z.Q.Liu, S.W.Zeng, M.Motapothula, S.Dhar, A.Ariando, Q.Wang, T.Venkatesan, *AIP Advances*, 2(1), (2012); <https://doi.org/10.1063/1.3682346>
- [33] N.Aghashahi, M.R.Mohammadizadeh, P.Kameli, *PhysicaScripta*, 97(4), (2022); <https://doi.org/10.1088/1402-4896/ac576b>
- [34] B.I.Shklovskii, A.L.Efros, B.I.Shklovskii, A.L.Efros, *Electronic properties of doped semiconductors*, 202-27(1984); [https://doi.org/10.1007/978-3-662-02403-4\\_9](https://doi.org/10.1007/978-3-662-02403-4_9)
- [35] M.N.Islam, S.K.Ram, S.Kumar, *Physica E: Low-dimensional Systems and Nanostructures*, 41(6), 1025-28(2009); <https://doi.org/10.1016/j.physe.2008.08.047>
- [36] R.Roy, A.Dutta, *Journal of Alloys and Compounds*, 843(2020); <https://doi.org/10.1016/j.jallcom.2020.155999>
- [37] C.Feng, J.Fei, K.Wen, W.Lv, Z.Zhang, M.Zou, F.Yang, M.Waqas, W.He, *Solid State Ionics*, 303(2017); <https://doi.org/10.1016/j.ssi.2017.03.007>
- [38] D.B.Strukov, R.S.Williams, *Applied Physics A*, 94(3), (2009); <https://doi.org/10.1007/s00339-008-4975-3>
- [39] X.Yan, J.Zhao, S.Liu, Z.Zhou, Q.Liu, J.Chen, X.Y.Liu, *Advanced Functional Materials*, 28(1), 1705320 (2018); <https://doi.org/10.1002/adfm.201705320>
- [40] P.Junsangri, F.Lombardi, *IEEE Transactions on Nanotechnology*, 12(1),71-80(2012); <https://doi.org/10.1109/TNANO.2012.2229715>
- [41] R.Mutlu, *European Journal of Engineering and Applied Sciences*, 1(1), 9-13(2018).
- [42] P.Bansal, B.Raj, *Journal of Nano engineering and Nano manufacturing*, 6(4), 306-12(2016); <https://doi.org/10.1166/jnan.2016.1296>
- [43] S.Shin, K.Kim, S.M.Kang, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 29(4), 590-598(2010); <https://doi.org/10.1109/TCAD.2010.2042891>
- [44] T.D.Dongale, K.P.Patil, P.K.Gaikwad, R.K.Kamat, *Materials Science in Semiconductor Processing*, 38 (2015); <https://doi.org/10.1016/j.mssp.2015.04.033>
- [45] F.Messerschmitt, M.Kubicek, J.L.Rupp, *Advanced Functional Materials*, 25(32), (2015); <https://doi.org/10.1002/adfm.201501517>
- [46] D.Biolek, J.Bajer, V.Biolkova, Z.Kolka, 2011 20th European Conference on Circuit Theory and Design (ECCTD) IEEE, 488-91(2011); <https://doi.org/10.1109/ECCTD.2011.6043393>
- [47] D.Biolek, Z.Biolek, V.Biolková, *Electronics Letters*, 50(2), 74-75(2014); <https://doi.org/10.1049/el.2013.3108>
- [48] S.Hamdioui, S.Kvatinsky, G.Cauwenberghs, L.Xie, N.Wald, S.Joshi, H.M.Elsayed, H.Corporaal, K.Bertels, *Design, Automation & Test in Europe Conference & Exhibition IEEE* 722(2017); <https://doi.org/10.23919/DATE.2017.7927083>
- [49] J.Singh, B.Raj, *Nanoscale Devices*,393(2018); <https://doi.org/10.1201/9781315163116-17>
- [50] S.P.Adhikari, M.P.Sah, H.Kim, L.O.Chua, *Three fingerprints of memristor. Handbook of Memristor Networks*, (2019); [https://doi.org/10.1007/978-3-319-76375-0\\_5](https://doi.org/10.1007/978-3-319-76375-0_5)

- [51] Y.Xu, J.Ma, X.Zhan, L.Yang, Y.Jia, Cognitive neurodynamics, 13(2019); <https://doi.org/10.1007/s11571-019-09547-8>
- [52] M.P.Sah, H.Kim, L.O.Chua, IEEE circuits and systems magazine, 14(1), 12-36(2014); <https://doi.org/10.1109/MCAS.2013.2296414>
- [53] A.Mazady, Modeling, fabrication, and characterization of memristors, (2014).
- [54] A.V.Fadeev, K.V.Rudenko, Russian Microelectronics, 50 (2021); <https://doi.org/10.1134/S1063739721050024>
- [55] X.Xiong, F.Xiong, H.Tian, Z.Wang, Y.Wang, R.Tao, L.H.Klausen, M.Dong, Advanced Electronic Materials, 8(2), 2022; <https://doi.org/10.1002/aelm.202100845>
- [56] T.Bunnam, A.Soltan, D.Sokolov, O.Maevsky, P.Degenaar, A.Yakovlev, IEEE 1-4 (2020); <https://doi.org/10.1109/SENSORS47125.2020.9278602>