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SPIN-ON DOPING (SOD) AND DIFFUSION TEMPERATURE EFFECT ON RE-COMBINATIONS/IDEALITY FACTOR FOR SOLAR CELL APPLICATIONS

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Diffusion process on different temperatures and related effects on ideality factor (*η)* and recombinations in solar cell have been investigated. Phosphorus-doped n+-emitters were fabricated by applying Spin-on doping (SOD). Dark current-voltage characterization has been used to investigate different recombinations and their relation with the ideality factor. Dark IV characteristics also revealed different current saturation limits at different diffusion furnace temperatures. Effect of doping temperature on sheet resistance helped to get optimized value at 950 °C to reduce carrier recombination and emitter recombination velocity in surface emitter layer. It was observed that there was strong dependency of sheet resistance over temperature in making n+-emitter layer of monocrystalline solar cells.

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1. Introduction

In a crystalline solar cell processing, diffusion of minority carriers into p-type or n-type wafers is a critical step to form an emitter. It requires uniform sheet resistance and low surface recombination velocity [1]. After diffusion, emitter sheet resistance can give a better idea about the diffusion profile. In solid doping sources one can tailor the diffusion profiles by changing the source concentrations [2], whereas in spin-on doping process temperature is the key factor to control diffusion profiles but sheet resistance value can be reduced to required value by using dilute HF [3]. So sheet resistance has direct relation with the diffusion, especially in spin-on doping. Series resistance is another important factor which is a function of grid geometry and can be calculated by assuming that resistance of the grid electrode is less than the sheet resistance [4]. Normally sheet resistance beneath the contact differs from the semiconductor sheet resistance beside the contact and low values of contact resistance are associated with heavy doping and vice versa. Contact resistivity can be calculated by the method $\boldsymbol{\rho_c} = R_s L^2_T$ where as L_T called current transfer length and semiconductor sheet resistance R_s can be calculated by using equation (1).

$$V = IR = \left(\frac{IR_s}{Z}\right)\left(S + 2L_T\right) \tag{1}$$

where, current is I, separation between contact pads is S and the width of the contact pad is Z [5]. So according to the above formula sheet resistance Rs has direct relation with voltage of the cell but the overall performance of actual silicon solar cell may be limited by other factors such as recombination's through bulk or surface and light trapping etc. [6, 7]. Although solid doping sources have some advantage over spin-on doping in the perspective of uniform sheet resistance [2] our experiment is based upon spin-on dopant process. Unfortunately in spin-on doping it is

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difficult to get uniform sheet resistance, but this effect can be reduced by using ultrasonic nozzles for uniform and precise spreading of spin-on dopant. Due to that reason small area samples have been used in our experiment. Sheet resistance of the doped layers was measured by using the four-point probe method [8].

2. Experimental Work

The tested 1.5 cm × 1.5 cm × 290 μm monocrystalline solar cells were fabricated on <100> oriented p-type polishing corporation of America wafers, one side is polished and the other side is lapped and the resistivity is 1 Ω. cm. The wafers were cleaned by standard Radio Corporation of America (RCA) method to remove oxide followed by a 20-sec dip in 10:1 H_2O:HF. After de-ionized water rinse and N_2 blow, dry wafers were placed in the oven for 10 min at 100°C to drive out moisture. Spinning process was carried out at room temperature. Approximately 15 drops of the spin-on dopant (phosphorous) were applied to the substrate spinning at 2000 rpm for 25 sec creating a dopant layer of 0.5 micron. The top surface area of the wafer was doped with Phosphorous type spin-on dopant P8545SF [2:1] to be N-type. After 10 min bake in oven at 100°C wafers were placed in a quartz tube furnace at 900°C, 930°C, 950°C, 980°C, 1000°C, 1050°C and 1100°C for 60 minute each. After that, sheet resistance was measured for each of the sample presented in table 1. Then the samples were loaded into thermal evaporator and aluminum evaporation was done at back of the wafer while silver was used for front metallization. To pledge ohmic contact as well as to improve the contact properties contact annealing was done at 400 °C for 20 min. The grid structure of solar cells consists of metal mask grid pattern with finger spacing of 600μm, and finger width of 300μm. After fabrication the device was analyzed using dark current–voltage (I–V) measurement.

3. Results and Discussion

Mostly industrial silicon solar cells doped with phosphorus n+-emitter layer have sheet resistance in the range of 40-50 Ω/sq. Low sheet resistance is normally chosen to get a low-resistance ohmic contact between the metallization and the emitter layer. Very high doping values normally predict that there would be an increase in carrier recombination and in emitter recombination velocity on surface of emitter layer.

Due to that reasons values of sheet resistance should be optimized to minimum recombination as far as improvement in solar cell efficiency. Sheet resistance values in table. 1 clearly show their dependency on the doping temperature.

Table 1. Investigated values of sheet resistance against time and temperature via spin-on doping process

Sample #	Process adopted	Temperature (°C)	Time (min)	Sheet Resistance (Ω/□)
1	Spin On Doping	900	60	108.000
2	Spin On Doping	930	60	69.1000
3	Spin On Doping	950	60	40.0000
4	Spin On Doping	980	60	18.6000
5	Spin On Doping	1000	60	12.2300
6	Spin On Doping	1030	60	10.5900
7	Spin On Doping	1050	60	10.2100
8	Spin On Doping	1080	60	10.0100
9	Spin On Doping	1100	60	10.0000

As clear variation can be seen when maximum and minimum sheet resistances were 108Ω/sq and 10Ω/sq achieved at temperature 900°C and 1100°C, respectively.

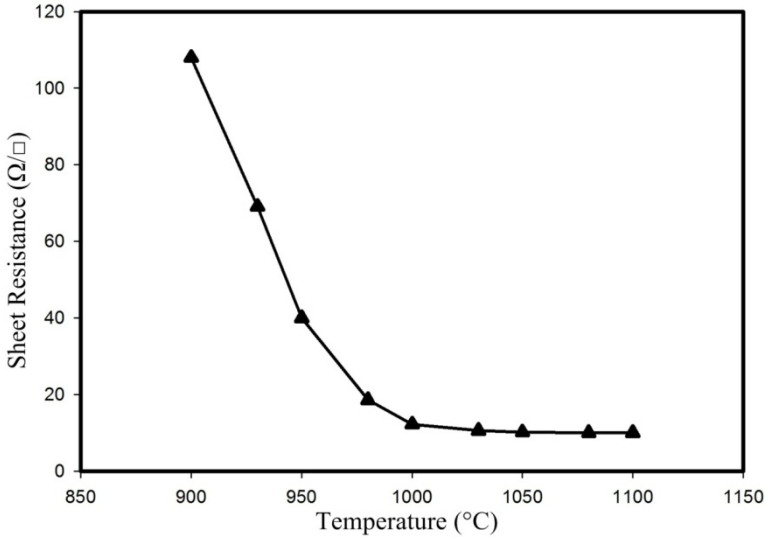

Fig. 1. Sheet resistance as a function of temperature for the samples prepared via spin-on doping process

It is clear from figure 1 that at temperature 900°C sheet resistance was 108 Ω/sq. As temperature increases to 950°C it decreases remarkably to 40 Ω/sq till temperature reached 1000 °C, the sheet resistance of the doped silicon wafer reaches to 12 Ω/sq. After that there was very little decrease in the sheet resistance has been noted. Until at 1100°C it reaches to10 Ω/sq, just 2 points decrease in 100 °C.

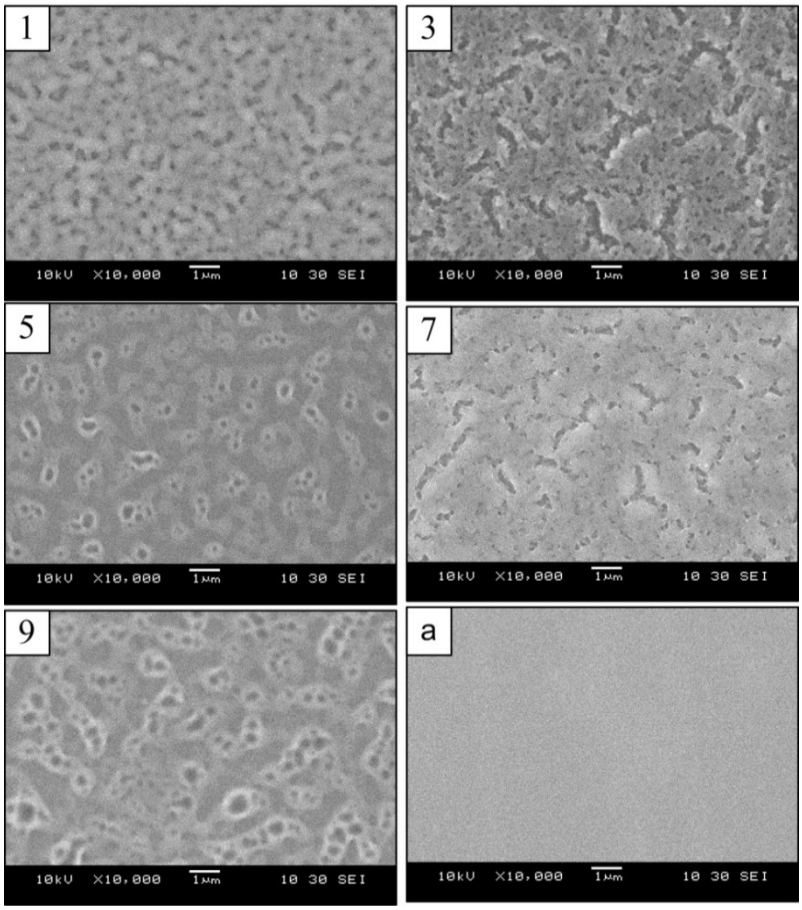

Fig. 2. Front surface SEM images (10kX magnification) of doped crystalline silicon each for 60 min., SOD at (1) 900°C, (3) 950°C, (5) 1000°C, (5) 1050°C, (7) 1100°C and (a) RCA cleaned un-doped c-silicon.

The SEM images in figure 2 show the comparison of front surfaces of the spin-on doped wafers at different temperatures. Figure 2(1) shows doping at 900°C, it has little patches while in figure 2(3) relatively large patches with deep penetration inside the wafer can be seen. In figures 2(5) and 2(9) medium sized patches only on the surface of the wafer were found. In figure 2(7) wafer doped by liquid phosphorous at 1050 °C showrelatively large patches on the upper surface. Figure (2) (a) shows the RCA cleaned front surface of the monocrystalline undoped wafer used in our experiment. Dark I-V characteristics reveal that there is diffusion temperature dependence of current saturation and also it is known that saturation current density J_{oe} varies with temperature [9].

From figure 3(a) it is clear that current saturates at higher voltage rather than the sample treated at higher temperature figure 3(b).

$$I = I_o\left[\exp\left(\frac{qV}{\eta kT}\right)-1\right] \tag{2}$$

At forward bias, the second term on the right side in Eq. (2) is neglected

$$I = I_o\left[\exp\left(\frac{qv}{\eta kT}\right)\right] \tag{3}$$

Changing equation 3 to semi-logarithmic scale yields

$$\ln I = \ln I_o + \ln\left[\exp\left(\frac{qv}{\eta kT}\right)\right] \tag{4}$$

$$\ln I = \left(\frac{q}{\eta kT}\right)V + \ln I_o \tag{5}$$

ln I_o = dark saturation current (recombination current) is the interception of the linear part of the semi-logarithmic plot at the y-axis. (I_1, V_1) and (I_2, V_2) are points taken within the region of interest in the curve where particular current mechanism dominates.
From Eq. (5) plotting *ln I* against *V* give,

$$Slope, m = \frac{q}{\eta kT} = \frac{\ln\left(I_2 / I_1\right)}{V_2 - V_1} \tag{6}$$

I_o is directly related to recombination, and thus, inversely related to material quality where *n* is called non-ideality factor ranging from 1-2, that increases with decreasing current also depend on the carrier transport mechanism [10]. Dark IV measurement shows the diode behaviour of prepared solar cells but the problem with the dark IV measurements is that current flows in the opposite direction of current paths. The change in the current path causes a lower series resistance. Saturation described in figure 3 has its origin in the body of the crystal and was not associated with contact phenomenon. Another factor was the barrier height which involves in dark characteristics such as a reduction of the potential barrier height increase the dark current and decreases the photocurrent.

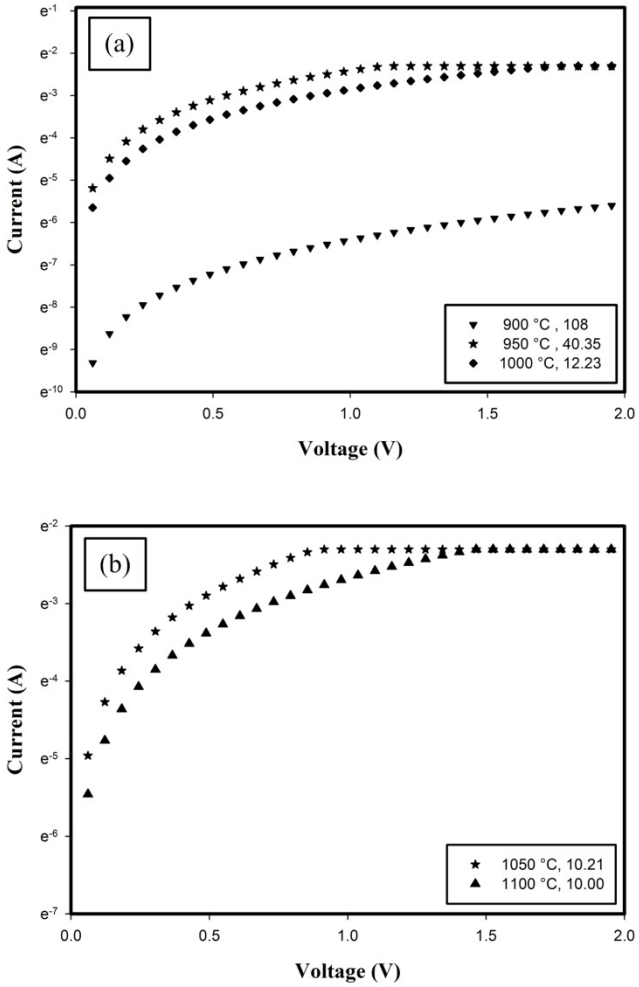

Fig. 3. Dark I–V (semi-logarithmic scale) characteristics of a P–N junction of c-silicon solar cell prepared via SOD process (a) at 900°C, 950°C and 1000 °C for 60 min (b) at 1050°C and 1100°C for 60 min.

Consequently, dark current increases by creating new paths and reduces the photocurrent since they can act as generation–recombination centres [11]. The ideality factor η can be determined from the slope of the I-V curve. By using Eq. 6 following equation has been derived to determine the ideality factor from the slopes of the figure 3.

$$\eta = \frac{q}{KT}\left[\frac{V_2 - V_1}{\ln\left(\frac{I_2}{I_1}\right)}\right] \tag{7}$$

Where, kT/q is the thermal voltage at 300 K (0.026 V), according to the ideal diode equation all the recombination occurs via band to band or recombination via traps in the bulk areas from the device (i.e. not in the junction). Ideal diode has ideality factor, η=1 which actually shows that how closely the diode follows the ideal diode equation. Recombination can also occur in another way and in different areas of the solar cell but these recombinations introduce ideality factors that may deviate ideality factor of the ideal diode as shown in table 2. In Shockley-Read-Hall recombination, for low level doping ideality factor 1 produces and that recombination is generally limited by minority carriers. While SRH recombination for high level doping have ideality factor 2, in which both minority and majority charge carriers participated. Auger recombination was most important in

heavily doped or heavily excited solar cells and in this process two majority and one minority carriers were involved which produces ideality factor 2 or 3. While in the depletion region (junction), two carriers were required for recombination and it has ideality factor 2. While figures 4 and 5 show the Raman spectra and XRD pattern of standard silicon p (100) wafer, used in the experiment.

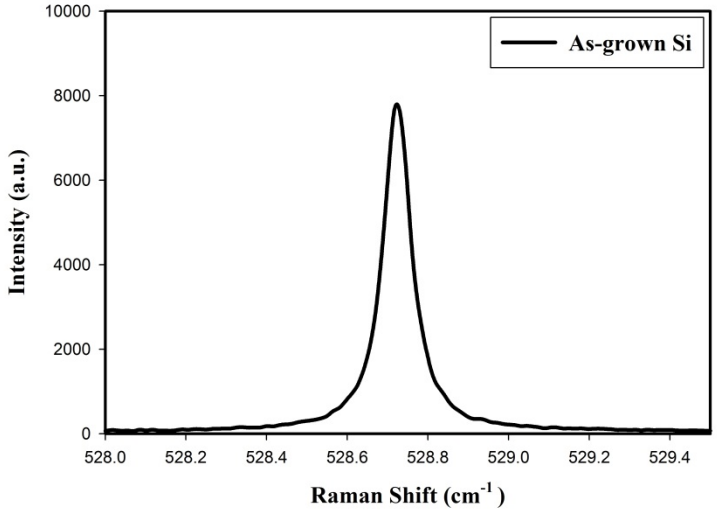

Fig. 4. Raman spectra of standard silicon p (100) wafer, used in the experiment.

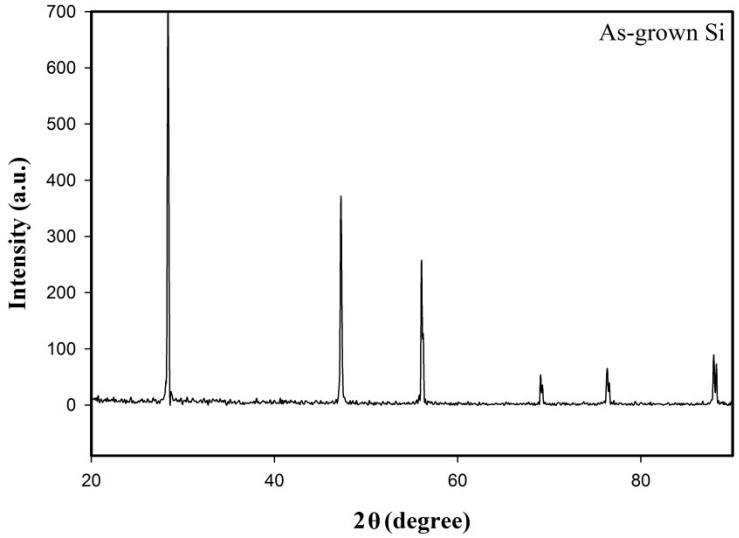

Fig. 5. XRD pattern of standard silicon p (100) wafer, used in the experiment.

Table 2. Ideality factors at different temperatures obtained by using dark I-V characteristics and equation no.7

Samples	Temperature (°C)	Ideality factor (η)
1	900	3.72
3	950	3.33
5	1000	3.38
7	1050	3.58
9	1100	3.37

4. Conclusion

In the perspective of formation of n+-emitter layer of monocrystalline solar cells at doping temperature 950°C was suitable for spin-on doped process. On that particular temperature ideality

factor was lowest (table 2). The value of sheet resistance was also very near to the optimized values of sheet resistance of industrial and laboratory monocrystalline solar cells. These optimized values are a helpful tool to reduce carrier recombination and emitter recombination velocity in surface emitter layer. But, there is still the need to optimize other factors involved in spin-on doping process, such as revolution per minute of spin-on coater, time and quantity of liquid phosphorous.

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References

[1] Z. Liu, Takato H, Togashi C, Sakata I, Applied Physics Letters **96**, 153503 (2010).
[2] T. Krygowski, Sana P, Crotty G, Rohaitg A. A novel technology for the simultaneous diffusion of boron, aluminum and phosphorus in silicon. 25th PVSC May 13-17-th, 396-393, 1996.
[3] A. Hiibner, Hampe C, Aberle A. G., Solar Energy Materials and Solar Cells **46**, 77-67 (1997).
[4] N. C. Wyeth,Solid-State Electronics **20**, 634-629(1977).
[5] D. L. Meier, Schroder D. K., Contact resistance: its measurement and relative importance to power loss in a solar cell. IEEE transactions on electron devices 653-647, May 1984.
[6] M. A. Green. Limits on the open-circuit voltage and efficiency of silicon solar cells imposed by intrinsic auger processes. IEEE Transaction On Electron Devices 678-671 May 1984.
[7] K. Ali, Khan S. A., MatJafri M. Z., Superlattices and Microstructures **52,** 782–792 (2012).
[8] J. Y. Lee. Boron back surface field using spin-on dopants by rapid thermal processing. Journal of the Korean Physical Society **44**, 1581-1586 (2004).
[9] P. Doshi, Rohatgi A. 18% Efficient Silicon Photovoltaic Devices by Rapid Thermal Diffusion and Oxidation. IEEE Transactions On Electron Devices August **45**, 1716-1710 (1998).
[10] W. Hamdi, J Mater Sci Mater Electron **8**, 409–418 (1997).
[11] C. Sah. Fundamentals of solid state electronics. USA: World Scientific Publishing, (1991).