OPTIMIZATION OF GRADED BANDGAP $Cd_{1-x}Zn_xTe$ THIN FILM SOLAR CELLS FROM NUMERICAL ANALYSIS

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Solar cells based on CdTe have reached a maximum practical recorded efficiency of 20.4%, which is low compared to its theoretical limit (29%). Novel concepts are required to further increase the efficiency of CdTe based solar cells. One possible approach is the graded bandgap CdZnTe solar cells. The commercial CdTe solar cells usually have thicker absorber layer. However, by using graded bandgap CdZnTe the absorber layer thickness can be reduced significantly, which eventually will reduce the cost, save processing time and energy required for fabrication. In this work, numerical simulation on graded bandgap CdZnTe solar cells is carried out by AMPS-1D software. The absorber layer of graded bandgap CdZnTe solar cells are optimized by two approaches (A and B), where each approach has four optimized structures. Finally, one optimized cell structure is selected for each approach. The results of the best cells for approach A and B are Voc= 0.884 Volt, Jsc= 32.074 mA/cm^2, FF= 0.801, Efficiency = 20.66% and Voc= 0.887 Volt, Jsc= 32.021 mA/cm^2, FF= 0.788, Efficiency = 20.35%, respectively. These cells have good stability at higher operating temperature, which are -0.043%/^{o}C for the best cell of approach A and -0.038%/^{o}C for the best cell of approach B. The best cells are also analyzed in terms of window layer thicknesses. It is found that by increasing the thickness of CdS window layer the efficiency decreases due to reduction of Jsc. Additionally, it is found that efficiency further increases for the insertion of a ZnO buffer layer.

1. Introduction

The sun is a free and infinite source of energy, which is one of the most significant types of the sustainable and renewable energy source. The direct conversion of the sunlight into electricity using solar cell is known as photovoltaic (PV) conversion. In PV technology, silicon is the most widely used material so far and it is still dominating the PV market [1, 2]. However, the manufacturing process of silicon based solar cells is still expensive. Therefore, thin film technology for solar cells becomes the subject of intense research at present.

One of the most promising thin film candidates is CdTe owing to its higher conversion efficiency with reduced material usage and stable cell operation [3,4]. CdTe solar cells have some advantages. Firstly, the layer of CdTe solar cells can be deposited using different low cost techniques such as Sputtering, Close-spaced sublimation (CSS), chemical bath deposition etc [5]. Secondly, CdTe has a direct optimum band gap (1.45eV) with the high absorption coefficient over $5×10^5$/cm [6,7], which means that the incident photons with sufficient energy can be absorbed within a few micrometers of CdTe absorber thickness [8,9]. The requirement of less material reduces relatively the cost of CdTe based solar cells. To date, the highest reported conversion

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efficiency of CdTe solar cell is 20.4% [10], which is still lower compared to the theoretical efficiency (near to 30%) [10]. One way to increase the efficiency of CdTe thin film solar cells are using graded bandgap $Cd_{1-x}Zn_xTe$ absorber layer [11]. The bandgap of $Cd_{1-x}Zn_xTe$ can be varied in the range of 1.45 eV to 2.2 eV, depending on the composition of Zn (x in $Cd_{1-x}Zn_xTe$). For example, the bandgap of $Cd_{1-x}Zn_xTe$ for x=0.1 is 1.56 eV [12]. By using graded $Cd_{1-x}Zn_xTe$ layer a wide spectral range can be covered for useful absorption in solar cells. The maximum efficiency of 7.2% is recorded for CdZnTe solar cells by co-sputtering of CdTe and ZnTe targets followed by annealing treatment at 520°C in pure H2/Ar ambient and then the process is continued in mixed vapor of CdCl2 +0.5% ZnCl2 in a H2/Ar ambient at 430°C [13]. Furthermore, the CdZnTe layer can also be used as the back contact for CdTe solar Cells [14]. The practical efficiency of CdZnTe solar cell is usually very low, which is likely due to the defects and chemical disorder of the CdZnTe layer [13]. Commercially available CdTe solar cells usually have thick absorber layer. To reduce the cost significantly, toxicity threat as well as to save the manufacturing time required for fabrication of solar cells maintaining high efficiency, ultra-thin absorber layer of graded bandgap $Cd_{1-x}Zn_xTe$ solar cells can be used [11]. This is because of their high absorption coefficient over 90% photon can be absorbed within 1μm thickness [16].

Simulation of graded bandgap CdZnTe solar cells by AMPS software is done in other literature [15]. The basic layers of ITO, CdS, and graded bandgap of CdZnTe material as an absorber layer with maximum 1.65 μm thickness is used [15]. Four best structures with efficiency more than 20% are found without any back contact. However, in this work, a back contact with φb= 1.25 eV [16] is used to make the cells more practically useful. In this paper, the absorber layer of graded bandgap solar cells are optimized following two approaches. Each approach has four optimized structures and finally one best cell was selected from each approach. The best cells are analyzed in terms of absorber layer and window layer thickness, buffer layer and operating temperature.

2. Methodology and Modelling of Novel Structures

The graded bandgap structure can be achieved in AMPS by inserting several thin layers of $Cd_{1-x}Zn_xTe$ as absorber, with each layer having the same properties except for its bandgap, which is varied from 1.45 eV up to 1.8 eV in steps of 0.05 eV [15]. The thicknesses of the layers are varied and their effects on the performance of the cell are analysed. Ideally, the layers should be infinitesimally small such that virtually no physical property alteration is observed between neighbouring layers. However, since AMPS is a numerical analysis tool, it divides the device into grids, placing a limit to the number of layers that can be used [19]. The maximum number of eight layers can be used as absorber. The optimization of absorber layer is performed in two ways, named as approach A and approach B. The material properties used for this simulation is given in Table 1 and 2. The back contact with barrier height φb= 1.25 eV is used and the operating temperature of the cell is 300K [20].

Table 1: Properties of the layers that are used in simulation [15,20]

Parameters	SnO$_2$	CdS	CdZnTe	ZnO
W[nm]	100,500	50,100	400,4000	100
$\varepsilon/\varepsilon_\circ$	9	10	10.20	9
$\mu_e[cm^2/Vs]$	100	100	250	100
$\mu_p[cm^2/Vs]$	25	25	70	25
n,p [cm^{-3}]	n:10^{17}	n:10^{17}	p:5×10^{14}	1.0×10^{18}
E_g[ev]	3.6	2.42	1.45 -1.8	3.3
N_c[cm^{-3}]	2.20×10^{18}	2.20×10^{18}	1.5×10^{17}	2.20×10^{18}
N_v[cm^{-3}]	1.80×10^{19}	1.80×10^{19}	1.80×10^{18}	1.80×10^{19}
χ_e [ev]	4.5	4.5	4.70	4

Table 2: Front and back contacts parameters used for simulation [16,15]

Φ_b [ev]	0.10	1.25
S_e [cm/s]	1×10^7	1×10^7
S_h [cm/s]	1×10^7	1×10^7
R_f	0.01	0.99

2.1 Approach A

In this approach, at first, TCO and window layers thickness are fixed at 100 nm. The CdZnTe absorber layer bandgap is varied from 1.8 eV to 1.45 eV with equal steps of 0.05 eV, while keeping the material properties unchanged. The highest bandgap (1.8 eV) of the absorber layer is named A, and in alphabetic order, the underlying layers are named B, C, D, E, F, G and H, respectively. In this approach, all eight absorber layers are inserted in AMPS with the thickness of 110 nm. Then the thickness of the top absorber layer (A) is varied from 30 nm to 110 nm in order to get the optimum thickness for obtaining the maximum efficiency. The optimized thickness of layer A is found to be 30 nm. The thickness of layer A is fixed to 30 nm and all the other layers are constant at 110 nm. Next, the thickness of layer B varied from 30 nm to 110 nm to find the optimum thickness. The optimized thickness of the layer B is found 30 nm. In this way, all the layers are optimized, and four different structures exhibiting maximum efficiency are found as shown in figure 1.
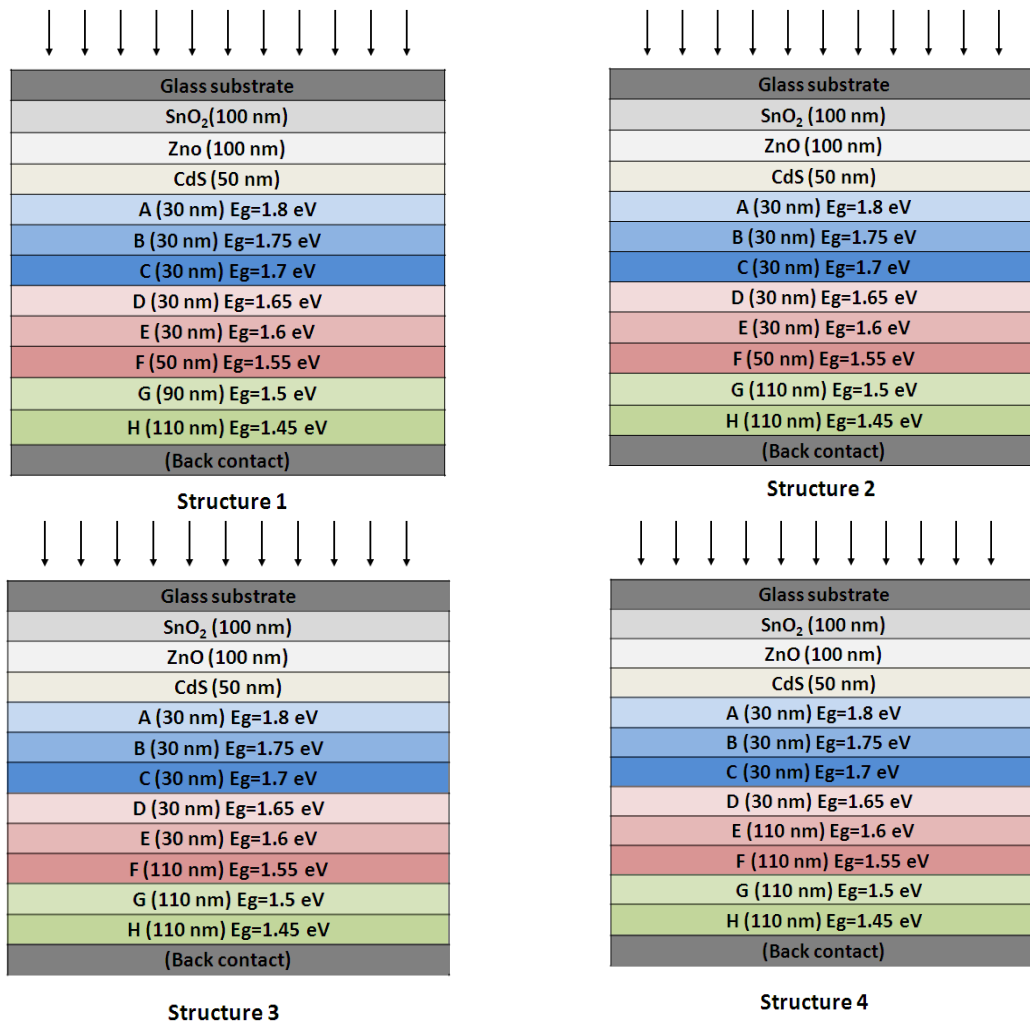

Fig. 1: Four different optimized structures following approach A (not to scale). The direction of the incident light is shown by arrows.

2.2 Approach B

In approach B, the thicknesses of TCO and window layers are fixed at 100 nm similar to approach A. Then layer A (Eg=1.8eV) is introduced on top of the window layer. Next, the thickness of layer A is varied from 30 nm to 110 nm and the optimum thickness is found to be 110 nm. Hence, the layer B is added to the layer A and the thickness is varied from 30 nm to 110 nm to find the optimum thickness of layer B. The optimized thickness is found to be 110 nm for this layer. In this way, the optimized thickness of layer C and layer D are found to be 110 nm and 70 nm, respectively, as shown in the structure 1 of figure 2. In the structure 2 of figure 2, one additional layer E is introduced. Similarly, layer F and G are introduced in the structures 3 and 4, respectively.
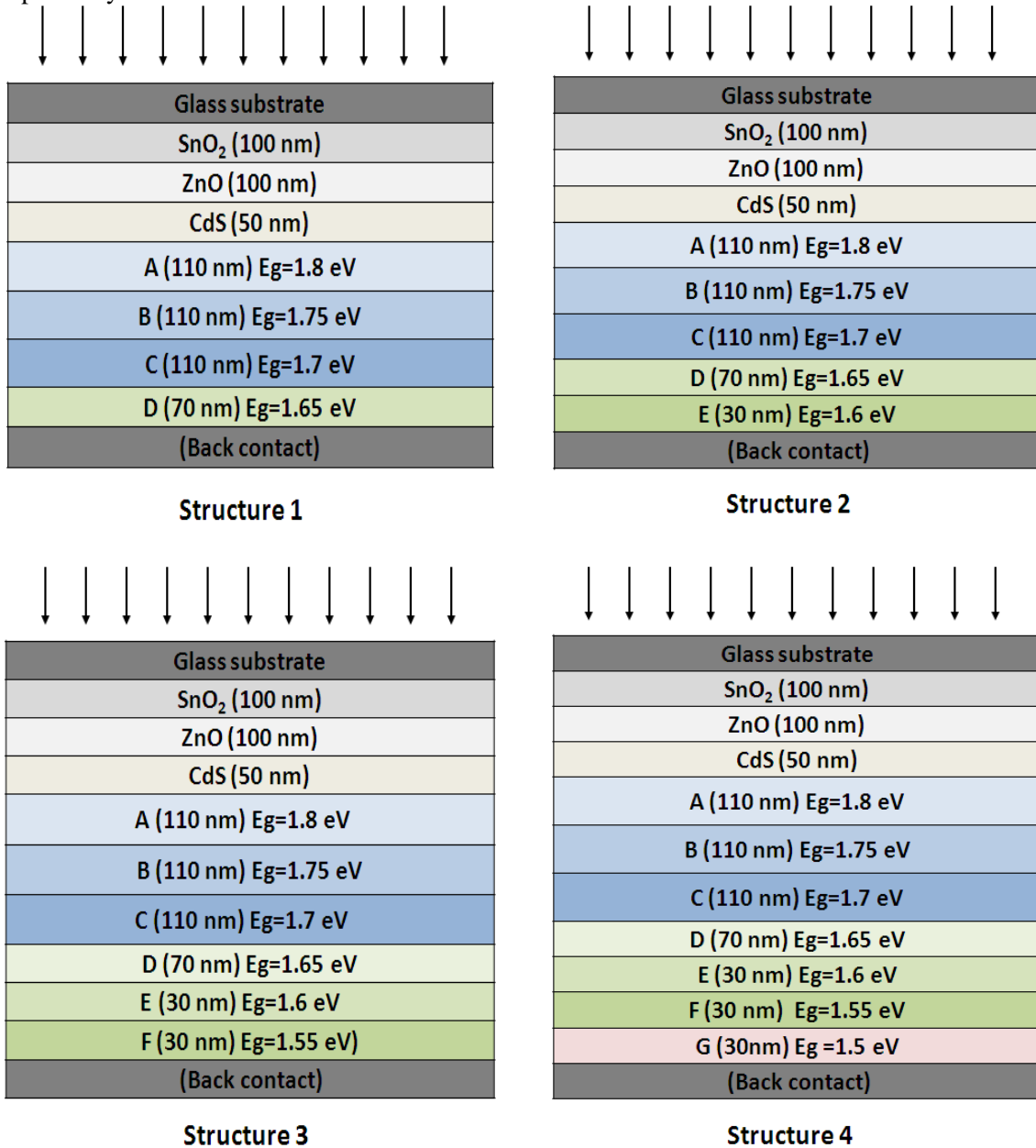
Glass substrate
SnO$_2$ (100 nm)
ZnO (100 nm)
CdS (50 nm)
A (110 nm) Eg=1.8 eV
B (110 nm) Eg=1.75 eV
C (110 nm) Eg=1.7 eV
D (70 nm) Eg=1.65 eV
(Back contact)

Structure 1

Glass substrate
SnO$_2$ (100 nm)
ZnO (100 nm)
CdS (50 nm)
A (110 nm) Eg=1.8 eV
B (110 nm) Eg=1.75 eV
C (110 nm) Eg=1.7 eV
D (70 nm) Eg=1.65 eV
E (30 nm) Eg=1.6 eV
(Back contact)

Structure 2

Glass substrate
SnO$_2$ (100 nm)
ZnO (100 nm)
CdS (50 nm)
A (110 nm) Eg=1.8 eV
B (110 nm) Eg=1.75 eV
C (110 nm) Eg=1.7 eV
D (70 nm) Eg=1.65 eV
E (30 nm) Eg=1.6 eV
F (30 nm) Eg=1.55 eV)
(Back contact)

Structure 3

Glass substrate
SnO$_2$ (100 nm)
ZnO (100 nm)
CdS (50 nm)
A (110 nm) Eg=1.8 eV
B (110 nm) Eg=1.75 eV
C (110 nm) Eg=1.7 eV
D (70 nm) Eg=1.65 eV
E (30 nm) Eg=1.6 eV
F (30 nm) Eg=1.55 eV
G (30nm) Eg =1.5 eV
(Back contact)

Structure 4

Fig. 2 Four different optimized structures following approach B (not to scale).
The direction of the incident light is shown by arrows.

3. Results and Discussion

3.1 Optimization of the Absorber Layer Thickness

Figure 3 shows the effect of each absorber layer thickness on performance parameters of the cells in approach A and B. Increase of the thickness of each absorber layer from 30 nm to 110 nm for the last three layers (F, G, and H) results in the short circuit current increase in approach A. However, for the first five layers (A, B, C, D and E) the decrease in short circuit current is insignificant, indicating a very little dependence on the layer thickness. The decrease in Jsc for the first five layers is due to reduced optical transmission of light to subsequent layers. However, for the last three layers, the absorption is lower compared to the top five layers, as most of the lights are absorbed by the top five layers. Hence by increasing the thickness of these bottom layers, more generation of carriers causes the increase in Jsc. In fact, the layer thickness influences the diffusion process of the carriers.

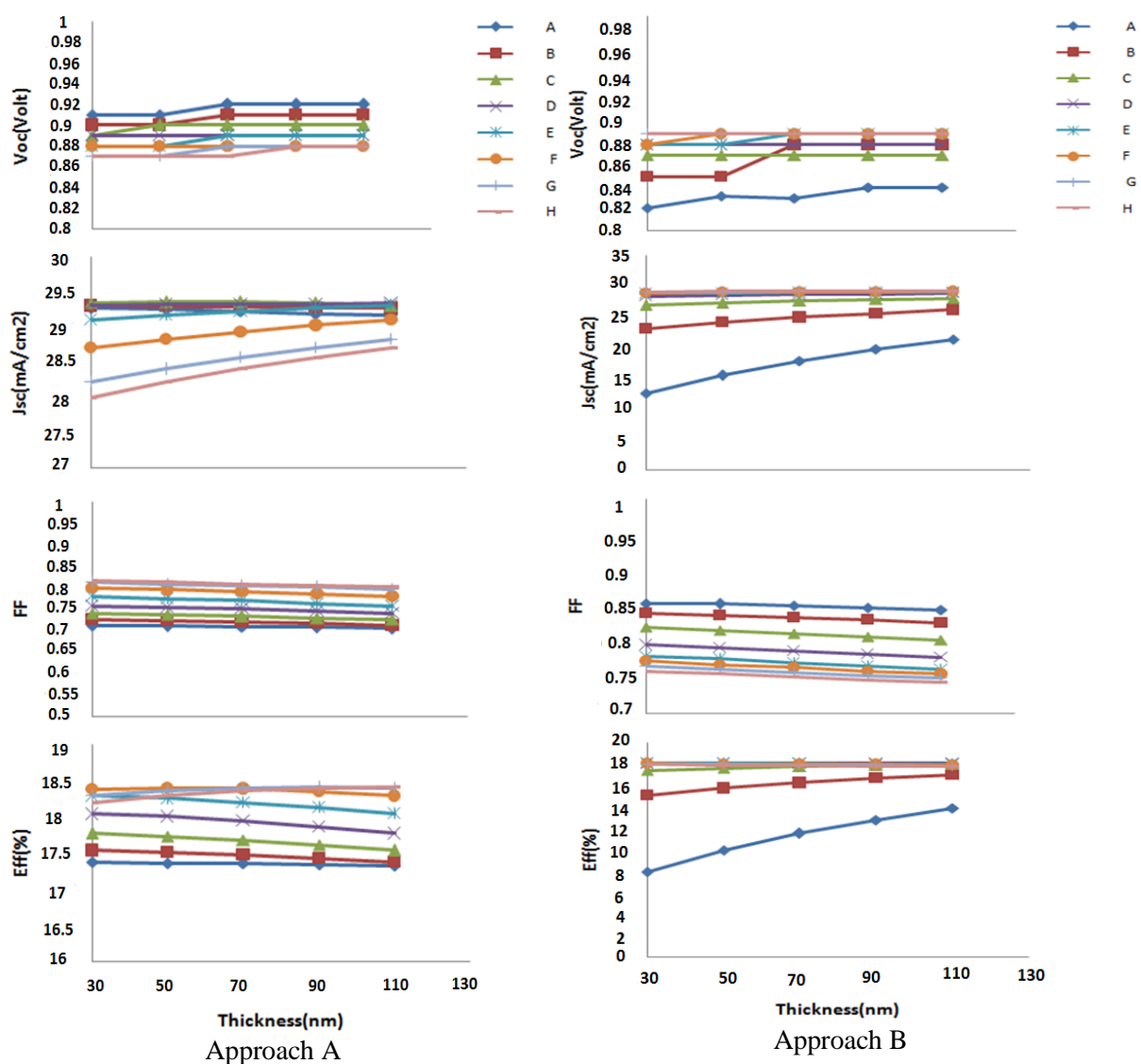Approach A   Approach B

Fig. 3: Different performance parameters of the cell as a function of the thicknesses of absorber layers for approach A and B

On the other hand, in approach B, the short circuit current increases at the increase of the thickness of each absorber layer for first three layers, and it is almost constant for the last five layers. This is because, there is only layer A in this approach at first. Therefore, by increasing the

thickness, the absorption as well as the current is also increasing. Similar phenomena are observed during the insertion of the layers B and C, respectively (as mentioned in approach B structure). As there are no other layers except for the first three layers, the thickness of the layers should be thicker to absorb the light enough into the layers and generate enough electron-hole pairs. Moreover, these layers are the nearest to p-n junction thus allow the effective conversion process. By adding last five layers respectively (D, E, F, G, H) to the first three layers, less light reaches to lower layers as the light has to pass through the first three thicker layers. Hence, the increase in current Jsc is not significant.

Figure 3 also shows the effect of each absorber layer thickness on open circuit voltage of the cell. In both approaches, the increase of the thickness of each absorber layer from 30 nm to 110 nm the open circuit voltage generally increases. This is due to overall increase of photo generation current. The effect of each absorber layer's thickness on fill factor (FF) of the cell is also shown. In both approaches, the increase of the thickness of each absorber layer from 30 nm to 110 nm reduces the fill factor, probably due to the increased series resistance.

In figure 3, the effect of each absorber layer's thickness on the efficiency of the cell for both approaches can also be observed. It shows that the thickness increase of layers A, B, C, D, E, from 30 nm to 110 nm decreases the efficiency of the cell in approach A, which is due to reduction of Jsc for these layers. However, the efficiency of layer F has not reduced significantly by increasing the thickness; which is likely an effect from the top five layers on layer F. The efficiency of the two last layers G and H increases with the increase in thickness; as the Jsc increases with thickness, so does the efficiency. However, the efficiency follows the trend of short circuit current Jsc for approach B. It means that the efficiency increases by increasing thickness of each absorber layer for the first three layers, and the efficiency is almost constant for the last five layers. The increase in short circuit current is due to the increasing thickness of layers. After optimization of all layers, four optimized structures are obtained for each approach. The output parameters of these optimized structures for approach A and B are shown in table 3.

Table 3: The performance of four optimized structures following approaches A and B

Approach A	V_{oc} (volt)	J_{sc} (mA/cm^2)	FF	Eff (%)	CZT thickness (nm)
Structure 1	0.88	28.713	0.801	18.411	400
Structure 2	0.88	28.833	0.796	18.405	420
Structure 3	0.88	29.106	0.78	18.293	480
Structure 4	0.89	29.314	0.758	18.046	560
Approach B					
Structure 1	0.88	28.656	0.787	18.132	400
Structure 2	0.88	28.824	0.78	18.127	430
Structure 3	0.88	28.956	0.773	18.093	460
Structure 4	0.89	29.059	0.766	18.039	490

3.2 Effect of CdS Window Layer Thickness

In this section, the effect of window layer thickness on the performance parameters of optimized structure (structure 1) is investigated for both approaches. CdS thickness is varied from 30 nm to 150 nm. Figure 4 shows that the Jsc and efficiency increases for the reduced thickness of CdS in both approaches. This is because the current losses below 510 nm wavelength region decrease by the reduced thickness of CdS. As a result, Jsc increases and thereby the efficiency

increases. It also shows that FF decreases due to the series resistance increase by the increased thickness of CdS. By optimizing the thickness of CdS from 100 nm to 50 nm, the efficiency has slightly increased from 18.411% to 18.482% for approach A and from 18.132% to 18.211% for approach B, respectively.
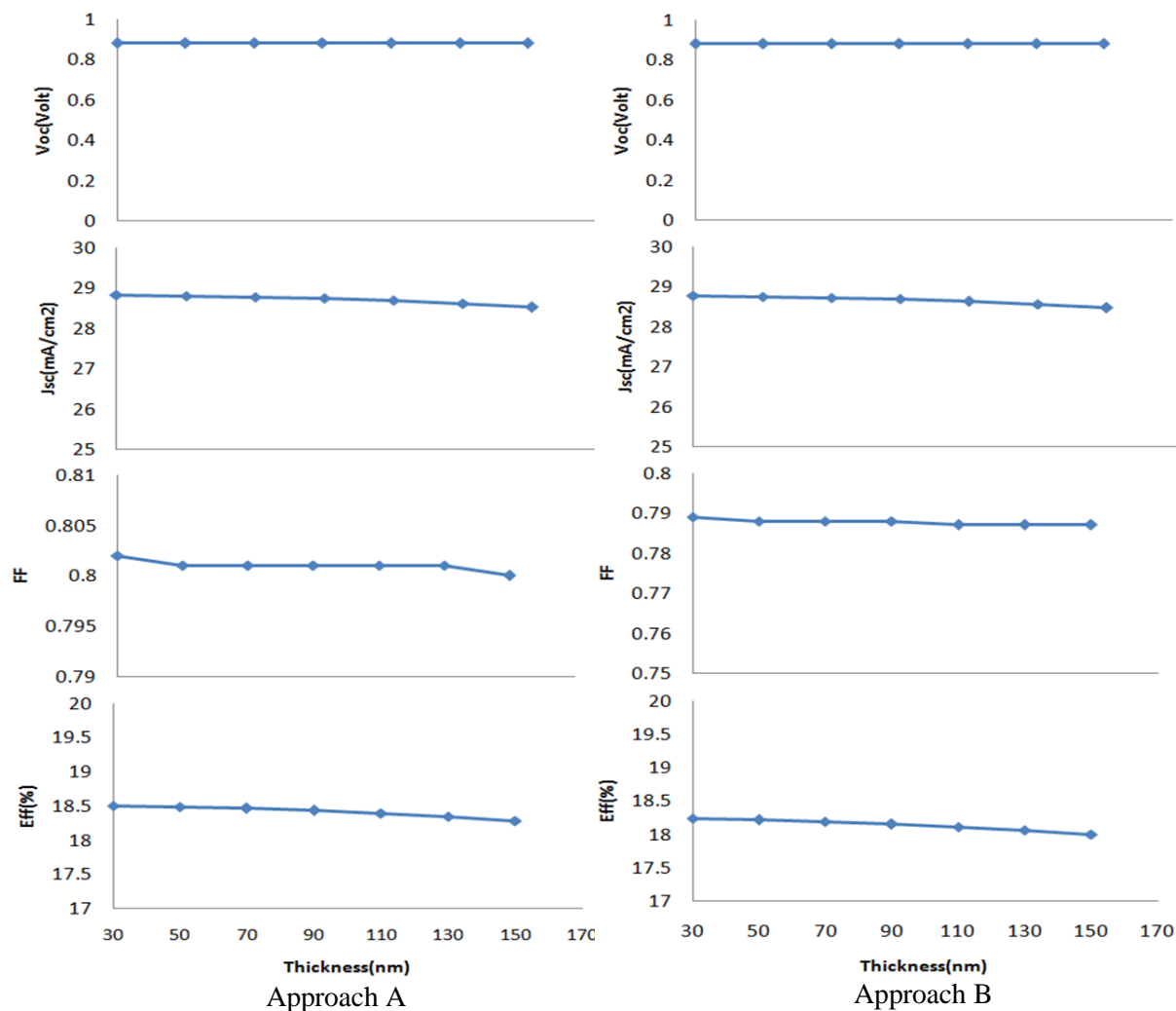

Fig. 4. Different performance parameters of the cell as a function of the window layer thicknesses for approach A and B

3.3 Effect of Buffer Layer

In this section we investigate the effect of buffer layer, which is in between window and front electrode, on the performance parameters of best optimized structure (structure 1) for both approaches. The thickness of the CdS window layer is selected as 50 nm. The large bandgap (3.3 eV) ZnO layer is used as a buffer layer in this case. In both approaches, by inserting a front buffer layer between window layer and TCO of the structure1, the efficiency and short circuit current of the cell increase. This is because the buffer layer is thin, highly resistive, highly conductive, which minimizes the forward leakage current and improves the film morphology of window layer by producing large grains during film growth [9]. Figure 5 shows the I-V characteristics of the best optimized structure (with CdS= 50 nm) of approach A and B with and without the front buffer layer.
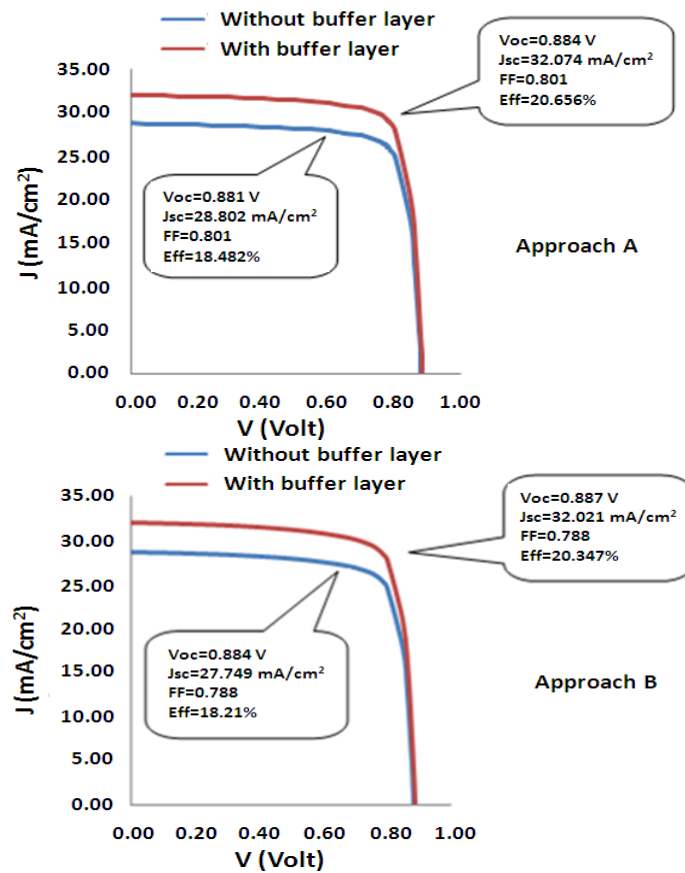
Fig. 5: I-V Characteristics of the best optimized structure (with CdS=50 nm)
following approach A and B, with and without front buffer layer

3.4 Effect of Operating Temperature

In this section, the temperature is varied from 300K to 400K. It is evident from the figure 7 that efficiency linearly decreases with operating temperature for both approaches. When the operating temperature increases the electrons in the solar cells gain extensive energy, but these electrons instead of contributing in the electricity become unstable and recombine with other holes, hence the short circuit current decreases. Moreover, the bandgap of semiconductor decreases due to the temperature rise, thus Voc also decreases and subsequently the efficiency [16]. For approach A, at T=300K and at T=400K, efficiencies are found to be 20.66% and 16.28%, respectively. Similarly for approach B, the efficiency of the best cell at T=300K and at T= 400 K are found to be 20.35% and 16.54%, respectively. The derived temperature coefficients are -0.043%/^{o}C and -0.038%/^{o}C for approach A and B, respectively, proving better stability of the cells at higher operating temperatur.
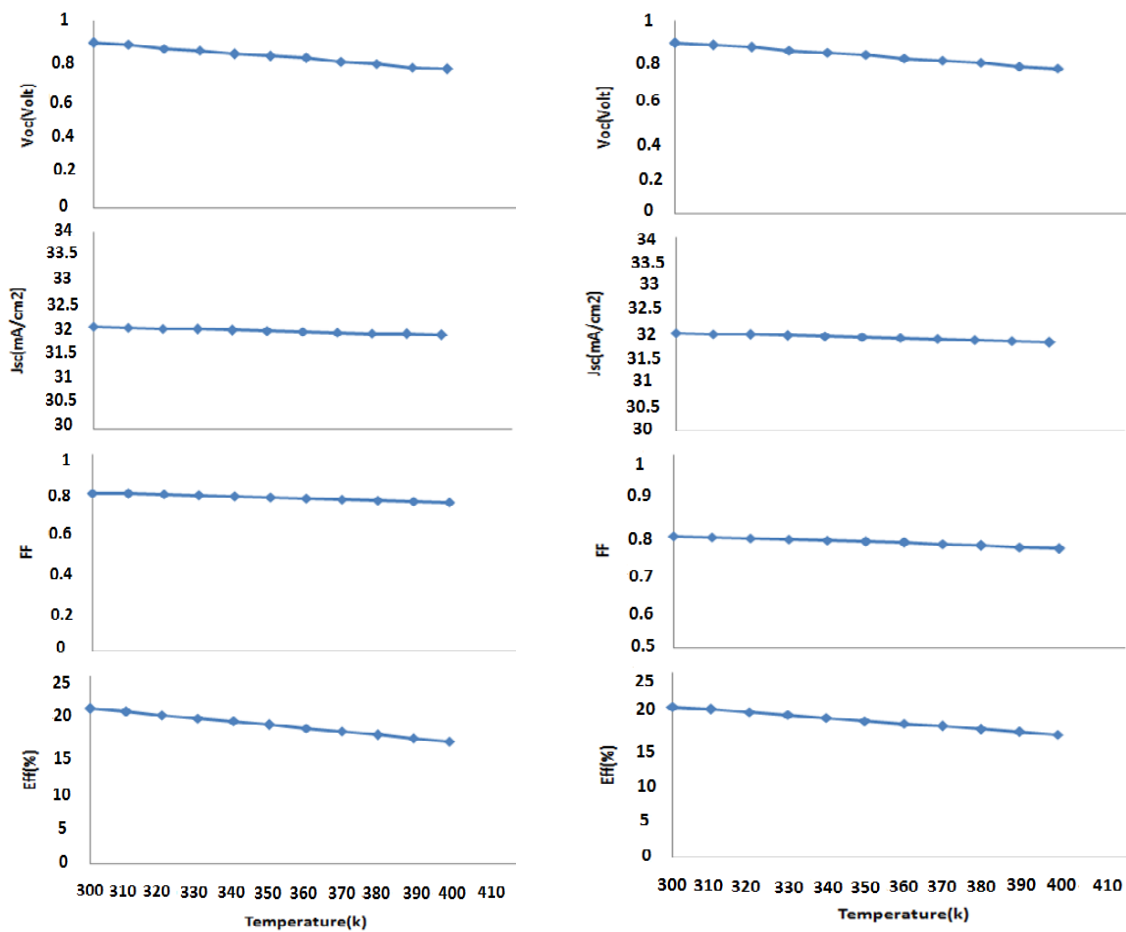
Approach A   Approach B

*Fig 6. The effect of temperature on performance parameters
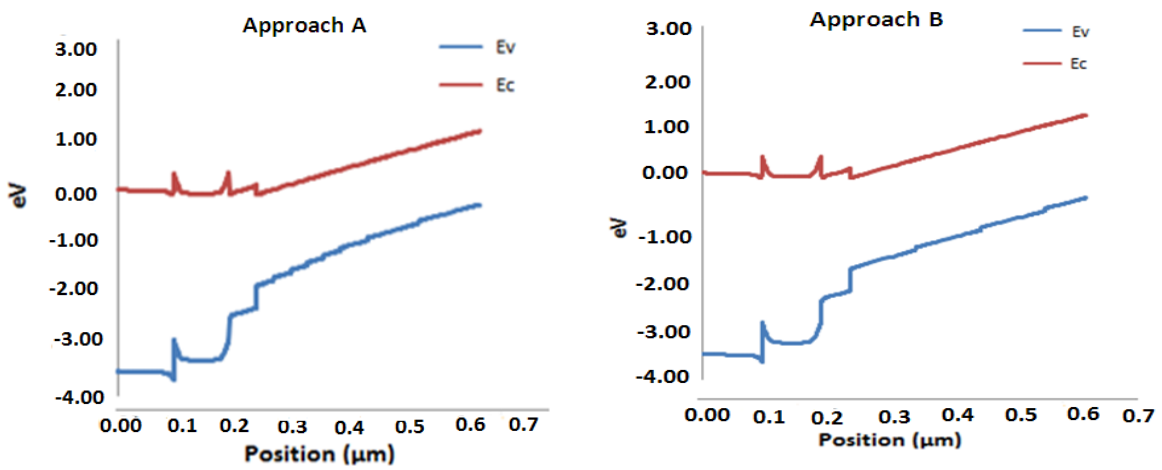of structure 1 in both approaches A and B*

Fig. 7. Band diagram profile of the best optimized structures (structure 1) for approach A and B

4. Conclusion

In this work, thin film CdZnTe absorber layer is proposed for solar cell. The CdZnTe absorber layer used in the numerical analysis has graded bandgap, which is varied between 1.45 eV to 1.8eV. Two approaches are investigated to find the best structure exhibiting maximum efficiency, where 4 layers of CZT films (structure 1) with varied bandgap are found to be the optimum in both cases. Both structures have equal total absorber layer thickness of 400 nm, but the thicknesses of individual absorber layers varied. The output parameters for the best cells in approach A and B are Voc= 0.884 V, Jsc= 32.074 mA/cm^2, FF= 0.801, Efficiency= 20.656% and Voc= 0.887 V, Jsc= 32.021 mA/cm^2 FF= 0.788, Efficiency= 20.347%, respectively. The high values of Jsc and Voc are attributed to higher bandgap of the absorber, strong electric field across the whole device as well as reduced conduction band offset and valence band discontinuity. Both structures show similar characteristics, exhibiting a relatively small temperature coefficient of -0.043%/^{o}C, for approach A and -0.038%/^{o}C for approach B indicating better stability of these structures at higher operating temperature. With these attractive performances, these structures have higher potentials to achieve higher practical efficiency solar cells.

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