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Mathematical modeling of various CdTe/CISSe based hetero-structure photovoltaic cells incorporating Si and CdS: using Scaps 1D simulator

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In this study, the primary focus was on enhancing the performance of Photovoltaic devices by modifying the ETL and HTL transport layers. We conducted a comprehensive analysis of efficiency and fill factor variations resulting from adjustments in key device parameters, notably the active layer` thickness. The HTL layer employed materials such as CdTe (Cadmium telluride) and CISSe (Copper indium sulfur selenide), while the ETL layer utilized CdS (Cadmium sulfide), ZnO (Zinc oxide), SnOx (Stannous oxalte), SnO_2 (Tin oxide), and TiO_2 (Titanium dioxide). Additionally, Silicon (Si) was incorporated into our structure. Our highest efficiency recorded was 27.38%, marking a significant achievement for our proposed cell design. In summary, our simulation results underscore the promising performance of the CdTe/CISSe/Si/CdS/ZnO structure, yielding an efficiency of 27.38%, an open-circuit voltage (V_{oc}) of 0.8136V, a short-circuit current density (J_{sc}) of 41.17428 mA/cm^2, and a fill factor (FF) of 79.36%. The discussions presented herein suggest that our proposed Photovoltaic (PV) Solar Cell holds great potential for adequate performance and improved power conversion efficiency, making it a compelling choice for solar energy applications.

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Keywords: CdTe/CISSe, CdS, Si, Heterojunction photovoltaic solar cell (HPSC), ETL, HTL, Efficiency

1. Introduction

Bangladesh, classified as a Least Developed Country (LDC), is home to nearly 169.82 million people as of 2022. Recently, the nation achieved a significant milestone in its power sector, boasting a power generation capacity of 25.5 GW, thereby granting over 97 percent of its populace access to electricity [1]. Despite these strides, Bangladesh faces challenges in optimizing its demand-side power generation, impeding its overall progress and development. The country heavily relies on fossil fuels such as natural gas, furnace oil, diesel, and coal for its electricity production. In the fiscal year 2022-23, natural gas dominated the energy mix at 50.32 percent, followed by furnace oil, diesel, and coal [2]. However, projections indicate that by 2028, Bangladesh's natural gas reserves will dwindle, threatening its energy security [3]. Compounded by population growth and diminishing non-renewable energy sources, rural communities bear the brunt of this energy imbalance, with urban areas consuming most available resources. To address this disparity and ensure sustainable energy access for rural populations, the adoption of clean, renewable, and affordable electricity production methods is imperative. By 2030, the nation aims to produce 4,100 MW of renewable energy, with contributions of 2,277 MW from solar, 1,000 MW from hydropower, and 597 MW from wind power. By 2041, Bangladesh targets sourcing 40% of its power from clean energy, while also planning to import 9,000 MW of renewable energy from neighboring nations [4].

Not only in the context of Bangladesh but worldwide solar energy emerges as a promising solution, offering potential cost reductions and widespread accessibility. Enhancing the efficiency of solar cells is key to realizing this vision, making research endeavors pivotal. Our research endeavors focus on designing and testing solar modules for optimal efficiency, leveraging simulations to refine setups and minimize shortcomings in physical implementations. At present,

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from the viewpoint of marketable context Si-based photovoltaic (PV) are the most universally reliable cells, and they render some proven steady features such as stable efficiency and unchallenging fabrication methods. However, beyond Silicon exploring alternatives allows researchers to push the boundaries of efficiency, cost-effectiveness, versatility, and sustainability in solar energy technology. Consequently, researchers are increasingly attracted to alternative photovoltaic (PV) technologies such as organic PV, hybrid organic-inorganic PV cells, dye-sensitized PV cells, perovskite PV cells, intermediate band gap solar cells, and low-dimensional hetero-structure-based PVs, all of which exhibit promising characteristics. For example, CdTe and CISSe are known for their relatively low production costs due to the abundance and low cost of the constituent elements and are both based on thin-film technologies, allowing for lightweight and flexible solar panels [5]. They have favorable absorption properties too [6]. As of the last update in January 2022, it's widely documented in scientific literature and news reports that CdTe solar cells have demonstrated high conversion efficiencies, with the current record exceeding 26%. CdS is often used as a buffer layer in CdTe-based solar cells, contributing to their efficiency enhancement [7][8].

In this research, we conducted a systematic examination of the physical, electronic, and optical characteristics of seven distinct types of heterojunction photovoltaic solar cells (HPSC). These cells were designed with appropriate holes and electron transport layers to ensure a suitable distribution of electric field. The structures are CdTe/CISSe/Si/CdS/ZnO, CdTe/CISSe/CdS/ZnO, CdTe/CISSe/CdS, CdTe/CISSe/CdS/SnOx, CdTe/CdS/SnOx, CdTe/CISSe/SnO_2/TiO_2, and CdTe/SnO_2/CdS respectively, basically based on employing the materials CdTe (Cadmium telluride) and CISSe (Copper indium sulfur selenide) as P-type layers while we utilized CdS (Cadmium sulfide), ZnO (Zinc oxide), SnOx (Stannous oxalte), SnO_2 (Tin oxide), and TiO_2 (Titanium dioxide) as N-type layers. The photovoltaic features of our proposed structures have been investigated by varying the layer thickness and doping level.

2. Structural modeling and simulation of proposed solar-cells

The methodology for designing the proposed solar cells, which incorporates basically CdTe, CISSe, Si, CdS and ZnO materials, using SCAPS-1D is elaborated in this section. The sequential steps comprising the entire procedure are delineated as follows. We observed how varying absorber thickness, doping concentration, absorber defect density, recombination rate (both radiative and band-to-band), as well as the influence of Electron Transport Layer (ETL), Hole Transport Layer (HTL), and back surface field, impacted the standard performance of our proposed configurations.

2.1. Simulation method for the devices

In this investigation, we utilize the widely adopted SCAPS-1D simulation software (version 3307) for modeling and simulation purposes. SCAPS-1D is a one-dimensional simulator that can handle up to seven semiconductor layers. It utilizes Poisson and Continuity equations to replicate different photovoltaic (PV) structures [9].

The software computes energy band structures, carrier concentrations, current densities, J-V characteristics, and spectral responses (quantum efficiency). It is widely used for simulating solar cell devices, demonstrating strong correlation with experimental findings. The simulations were carried out under standard conditions of 1.5 AM solar irradiance and at a temperature of 300 K.

2.2. Structural details of the proposed devices

Figure 1 displays the optimized structure of one of the seven proposed solar cells which is basically a PIN type structure. In this optimized proposed structure, a CdS is inserted as n-type (20 nm) ETL, ZnO is added as n-type transparent conducting layer (25 nm) at the top, while Si is proposed as an intrinsic type of absorber (optimized at 200 nm) layer. Then the p-type CISSe (50 nm of thickness) is added above the absorber layer combining with p-type CdTe (optimized at 3 μm) on the top as HTL and to provide as a back surface field. We investigated the same structure by eliminating the Si layer to see the impact of it on overall performance. The list of all the other examined structures to find the best cell efficiency is displayed in Table 1.

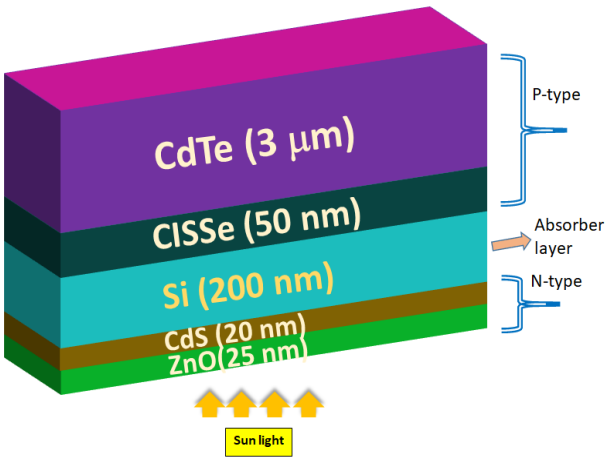

Fig. 1. (a) Schematic depiction of the best proposed heterojunction photovoltaic solar cell (HPSC) [PIN type: CdTe/CISSe/Si/CdS/ZnO] (structure 1, listed in table 1) in order to generate suitable performance features.

Table 1. The list of solar cell structures investigated for this research to simulate using SCAPS-1D

Structure Type	A few proposed Photovoltaic cells for simulation
Structure 1 (PIN type)	CdTe/CISSe/Si/CdS/ZnO
Structure 2 (PN type)	CdTe/CISSe/CdS/ZnO
Structure 3 (PN type)	CdTe/CISSe/CdS
Structure 4 (PN type)	CdTe/CISSe/CdS/SnOx
Structure 5 (PN type)	CdTe/CdS/SnOx
Structure 6 (PN type)	CdTe/CISSe/SnO_2/TiO_2
Structure 7 (PN type)	CdTe/SnO_2/CdS

2.3. A few suitable options for electron/hole-transport (ETL/HTL) and absorbers layer

The presence of electron/hole-transport materials (ETL/HTL) within photovoltaic (PV) cells plays a critical role in extracting photo-generated excitons from the absorber layer and directing them towards the outer connections. The careful selection of ETL and HTL is essential for facilitating active carrier transport at the interface, primarily dictated by the energy band configuration. The ETL facilitates electron transport while impeding hole movement, whereas the HTL facilitates hole transport while hindering electron flow [10]. Commonly encountered ETL materials in solar cells include Fe_2O_3, SnO_2, ZnO, TiO_2, SnOx, and In_2O_3. Among these, ZnO stands out as the most frequently utilized ETL due to its appealing attributes such as affordability, high electron mobility, low Eco toxicity, and stability [11][12]. The predominant materials for HTL include PEDOT:PSS, P3HT, and PTAA. Additionally, copper-based compounds like CuSCN, CuI, Cu2O, CuOx, and MoOx are being considered for their enhanced hole mobility, chemical robustness, and reasonable fabrication costs [13][14]. CISSe has recently emerged as a good choice for HTL applications.

Additionally, the integration of efficient absorber layers into heterojunction cells, along with the precise alignment of their energy bands with transport layers, is crucial for optimizing carrier dynamics and collection at metallic contacts. This alignment is achieved by ensuring that the work

function of the front contact material closely matches or slightly exceeds the conduction band edge of the transport layer [15]. As a result, a higher work function usually leads to an ohmic contact for holes and an electrostatic barrier for electrons within the Hole Transport Layer (HTL). Inadequate management of recombination mechanisms can result in performance decline, as accumulated charges interfere with the electric field within the cell. Therefore, ensuring proper alignment of Electron Transport Layer (ETL), Absorber, and HTL layers is crucial for maintaining consistent current flow throughout the entire Tandem architecture. Taking these considerations into account, Silicon was selected as a thin intrinsic (I) layer due to its abundant availability and established properties [16].

Table 2. The list of materials selected for ETL and HTL and their pertinent parameters [17][18][19][20].

Parameters	**CdTe**	**CISSe**	**CdS**	**ZnO**	**SnO_2**	**TiO_2**	**SnOx**
Bandgap (eV)	1.5	1.04	2.45	3.3	3.5	3.2	3.6
Electron Affinity (eV)	3.9	4.3	4.45	4.1	4.0	4.1	4.0
Dielectric permittivity	9.4	12.0	10.0	9.0	9.0	9.0	9.0
CB effective density of states ($1/cm^3$)	$8.0x10^{17}$	$1.0\ x10^{19}$	$2.0\ x10^{18}$	$4.0\ x10^{18}$	$2.2\ x10^{17}$	$2.2\ x10^{18}$	$2.2\ x10^{18}$
VB effective density of states ($1/cm^3$)	$1.8\ x10^{19}$	$1.0\ x10^{19}$	$1.5\ x10^{19}$	$1.0\ x10^{19}$	$2.2\ x10^{16}$	$1.0\ x10^{19}$	$1.8\ x10^{19}$
Electron thermal velocity (cm/s)	$1.0\ x10^{7}$	$1.0\ x10^{7}$	$1.0\ x10^{7}$	$1.0\ x10^{7}$	$1.0\ x10^{7}$	$1.0\ x10^{7}$	$1.0\ x10^{7}$
Hole thermal velocity (cm/s)	$1.0\ x10^{7}$	$1.0\ x10^{7}$	$1.0\ x10^{7}$	$1.0\ x10^{7}$	$1.0\ x10^{7}$	$1.0\ x10^{7}$	$1.0\ x10^{7}$
Electron mobility (cm^2/Vs)	$3.2\ x10^{2}$	$1.0\ x10^{2}$	$5.0\ x10^{1}$	$1.0\ x10^{2}$	$2.0\ x10^{1}$	$2.0\ x10^{1}$	$1.0\ x10^{2}$
Hole mobility (cm^2/Vs)	$4.0\ x10^{1}$	$2.5\ x10^{1}$	$2.0\ x10^{1}$	$2.5\ x10^{1}$	$1.0\ x10^{1}$	$1.0\ x10^{1}$	$2.5\ x10^{1}$
Shallow uniform donor density N_D ($1/cm^3$)	0	0	$1.0\ x10^{16}$	$1.0\ x10^{17}$	$1.0\ x10^{17}$	$1.0\ x10^{16}$	$1.0\ x10^{17}$
Shallow uniform acceptor density N_A ($1/cm^3$)	$1.0\ x10^{18}$	$1.0\ x10^{17}$	0	0	0	0	0

3. Results and discussions

A successful heterojunction photovoltaic solar cell (HPSC) requires meeting several criteria: ensuring proper matching of currents across adjacent junctions, achieving rapid separation of electron-hole pairs across a wide range of solar irradiance, and minimizing electrical resistance and photonic losses. These requirements can be managed by adjusting band-gap, thickness, and incorporating appropriate transport layers with suitable affinity levels [21][22].

It is established that photovoltaic cells generally exhibit higher efficiency when light enters the cell through a window layer with a higher band gap [23] . We proposed both PN and PIN type structures in this investigation. At first we designed six different types of PN heterojunctions as listed in Table 1. The structures are CdTe/CISSe/CdS/ZnO, CdTe/CISSe/CdS, CdTe/ CISSe/CdS/SnOx, CdTe/CdS/SnOx, CdTe/CISSe/SnO_2/TiO_2, CdTe/SnO_2/CdS. In all these structures CdTe and CISSe have been introduced as P-type layers. The CdS, SnOx, SnO2, TiO2, or ZnO are used as N-type. Then, we proposed our PIN type structure and selected CdS as the N-type window layer. An N-type ZnO has been added as Transparent Conducting Layer (TCO) in

combination with the CdS in this PIN HPSC. We have chosen CdTe and CISSe as the P-type layers which absorb the lower energy of photons of the solar spectrum and in addition, the CdTe supports the structure as a back surface field. The intrinsic (I) layer serves as an extra absorber, capable of capturing multiple near-infrared photons owing to its increased thickness, thereby providing a higher illumination current [24][25]. We have chosen Silicon (Si) as the I-layer due to its remarkable acceptability in terms of cost, availability, and durability [26]. Then again, the widest p-type-CdTe absorbs most of the carriers due to its extended area. By this overall construction, the photo-generated excitons experience the built-in electric field and run towards the outer contact. To observe the effectiveness of the proposed cell, thickness, doping densities, and defect-states of all layers are anticipated as key design parameters. Therefore, we investigated our structures by varying such parameters.

Calculating the Cell Power Conversion Efficiency (PCE) can be a complex task. Traditionally, it involves conducting a current-voltage (J-V) sweep under specific sunlight conditions, typically 1000 W/m^2 illumination at AM1.5G. This generates a curve, where the open-circuit voltage (V_{oc}) is where it intersects the voltage (x-axis), and the short-circuit current (J_{sc}) is where it intersects the current (y-axis). Examining the typical J-V curve reveals that the solar cell's characteristics aren't square, indicating that the power extracted from the device is less than the product of V_{oc} and J_{sc}. Instead, the focus shifts to finding the maximum power point (P_{max}), where voltage and current yield the highest extracted power. However, the voltage and current at this point aren't practical parameters for characterizing solar cells. To tackle this issue, a metric called the fill factor (*FF*) is introduced to connect these parameters with V_{oc} and J_{sc}. *FF* indicates the available power at the maximum power point, divided by V_{oc} and J_{sc}. Together, *FF*, V_{oc}, J_{sc}, and PCE serve as the primary performance metrics for evaluating solar cells. Improving efficiency involves enhancing the *FF*, V_{oc}, and J_{sc} of the device.

3.1. J-V curve of our proposed structures

At first we conducted simulation to examine the performance features, typically the J-V curve and quantum efficiency of our six PN type HPSC structures (Structure 2 to structure 7, as listed in Table 1, all are without the inclusion of silicon). We are exemplarily showing the J-V curve of two HPSC structures (CdTe/CdS/SnOx and CdTe/CISSe/CdS) in Fig. 2. The simulation results of CdTe/CISSe/CdS/ZnO as depicted in Fig. 3 reveal that by adding ZnO as TCO above the CdTe/CISSe/CdS HPSC structure offers the best features among the six proposed structures having the efficiency of 20.1%, V_{oc} of 0.8116 V, J_{sc} of 30.98mA/cm^2, and *FF* of 83.35%, respectively. From Fig. 3 it is evident that if the CdS is replaced by SnO_2 while the TCO is replaced by TiO_2, the efficiency is compromised by around 2%.

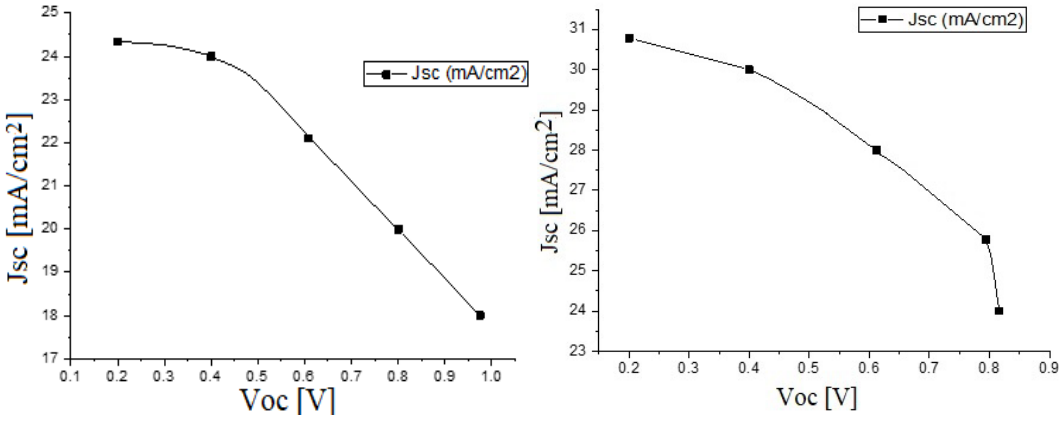

Fig. 2. J-V curve of (a) CdTe/CdS/SnOx and (b) CdTe/CISSe/CdS HPSC structures.

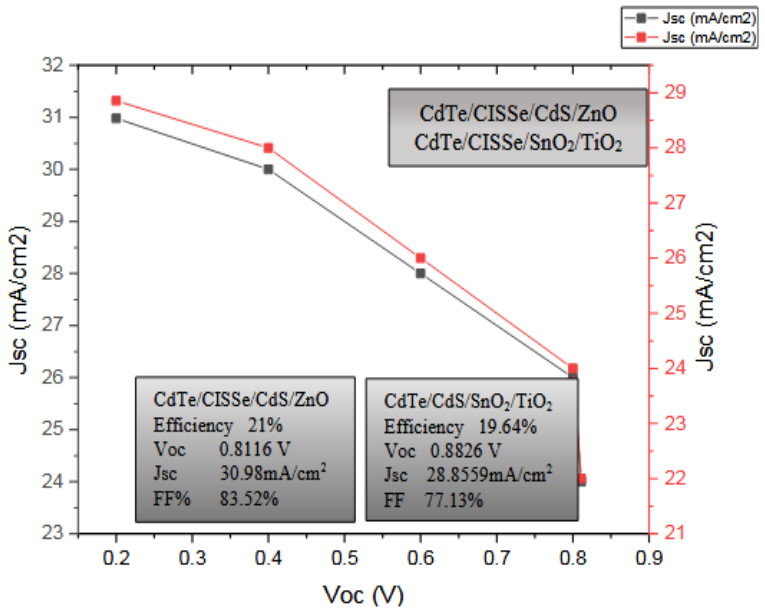

Fig. 3. The comparison between the J-V curve of (a) CdTe/CISSe/CdS/ ZnO and (b) CdTe/CdS/SnO_2/TiO_2 HPSC structures.

3.2. Influence of electron transport layer (ETL) thickness on the performance of PN type HPSC

The thickness of the ETL is crucial for the device's effectiveness. A thicker ETL results in increased series resistance and absorption losses within the device [27]. Given that light penetrates the device via the ETL, it necessitates high transparency along with an appropriate Forbidden gap and thickness. As an exemplification we have shown the variation of thickness of CdS as ETL on the performance parameters for the structure of CdTe/CISSe/CdS in Fig. 4. This analysis helped us to determine the optimum thickness of ETL layer in our proposed structures. We observe from Fig. 4 that as the thickness of CdS varies from 1 to 15 nm, the V_{oc}, J_{sc}, *FF* and the efficiency increases linearly. Between 15 nm to 50 nm the parameters exhibit slower increment and after 50 nm of -thickness the parameters start saturating. Therefore, it can be comprehended that 10 to 50 nm thickness can be a suitable choice for thickness selection of ETL layer.

In addition to this, for a better understanding a variation of the thickness of SnO_2 and TiO_2 on the performance of CdTe/CISSe/SnO_2/TiO_2 (Structure 6) and the variation of thickness of CdS and ZnO on the performance parameters (V_{oc}, Efficiency, J_{sc} and *FF*%) for the structure of CdTe/CISSe/CdS/ZnO (Structure 2) are displayed in Fig. 5. It is worth mentioning that SnO_2 has been used as ETL while TiO_2 is used as TCO in Structure 6. Similarly, CdS has been used as ETL and ZnO has been utilized as TCO for the Structure 2. We can see that for every layer, the performance parameters increase abruptly as the thickness is increased from 1 nm to 15 nm. From 15 to 100 nm the parameters increase slightly and after 100 nm very insignificant changes are noticed. However, among them for ZnO a conspicuous change in every performance metrics have been noticed between 15 to 100 nm from Fig. 5. After synergic optimization we observed that when CdS/ZnO are used combinedly, a 20 nm of CdS and a 25 nm of ZnO offers best efficiency for the Structure 2, which is 21.06%.

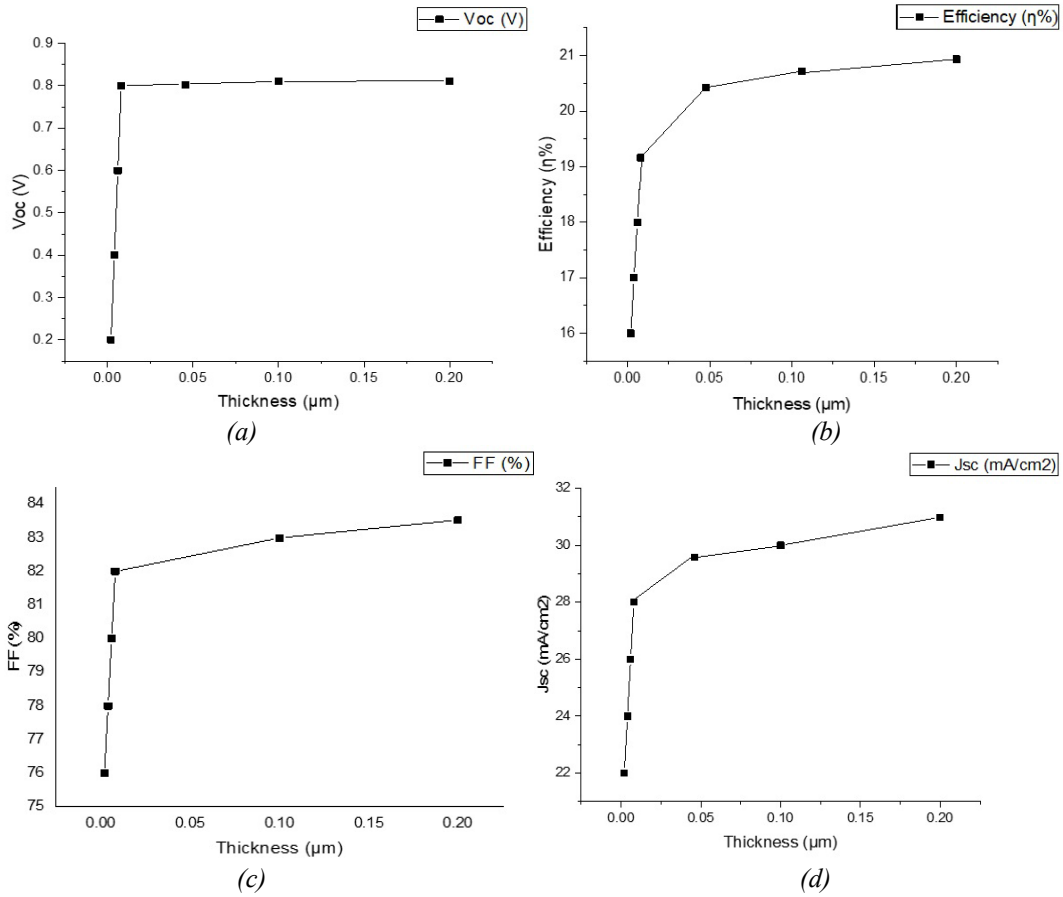

Fig. 4. The variation of thickness of CdS as ETL on the performance parameters (V_{oc}, efficiency, J_{sc} and FF%) for the structure of CdTe/CISSe/CdS.

3.3. Influence of Hole Transport Layer (HTL) Thickness on the performance of PN type HPSC

Hole-transporting layers (HTLs), sometimes referred to as anode interfacial layers, play a crucial role in extracting and transporting holes while preventing the flow of electrons. These layers, comprised of hole-transport materials, are strategically placed between the photoactive layer and the anode, enhancing the overall performance of the device [28]. For the sake of synergic optimization, the variation of thickness of HTL has also been performed for all structures. Since after synergic simulation, structure 2 has been obtained as the best HPSC in terms of efficiency, we are showing the variation of cell performance for this particular structure 2 (CdTe/CiSSe/CdS/ZnO) in Fig. 6. In the case of HTL we find out that less than 500 nm of thickness this layer could not offer requisite electric field to extract hole. From Fig. 6 it is clearly seen that the performance of the cell starts increasing after the thickness of HTL is increased beyond 1 μm. Particularly from the variation of open circuit voltage versus thickness of CdTe (HTL) curve we can recognize that the V_{oc} linearly increases with the increase of thickness which is quite typical for a P-type layer having smaller band gap; as we know smaller bandgap is associated with longer absorption length and therefore require larger thickness for complete absorption of photons having longer wavelength. Hence, we selected the thickness of CdTe as 3 μm to achieve the highest possible efficiency.

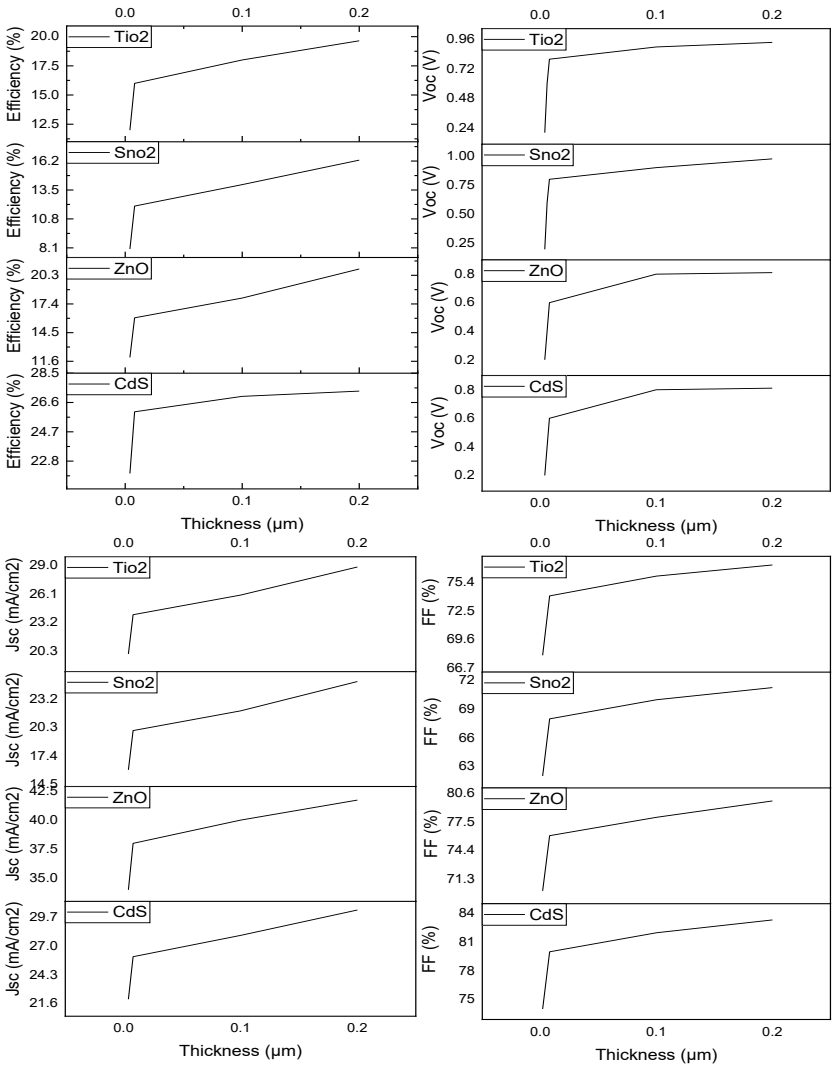

Fig. 5. The variation of the thickness of SnO_2 and TiO_2 on the performance of CdTe/CISSe/SnO_2/TiO_2. The variation of thickness of CdS and ZnO on the performance parameters (V_{oc}, efficiency, J_{sc} and FF%) for the structure of CdTe/CISSe/CdS/ZnO.

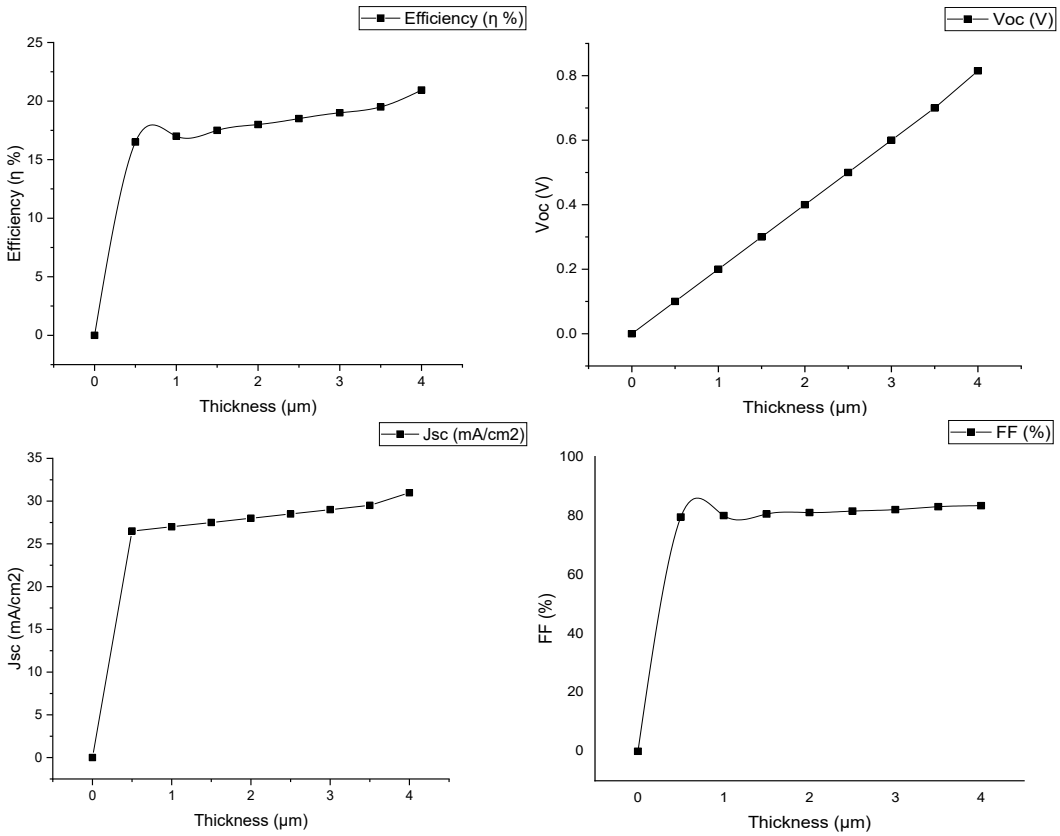

Fig. 6. The variation of the thickness of CdTe on the performance parameters (V_{oc}, efficiency, J_{sc} and FF%) for the structure of CdTe/CISSe/CdS/ZnO.

3.4. The proposed high performance PIN type HPSC with silicon as absorber

After rigorous optimization efforts, we have successfully developed a High Performance PN type HPSC, which is the structure 2 (CdTe/CISSe/CdS/ZnO). Then we attempted to produce a PIN type solar cell structure based on this above PN type solar cell so that we can further exceed the cell efficiency. Why did we choose silicon for our photovoltaic (PV) cells? Simply put, silicon-based solar cells offer a remarkable balance of high efficiency, affordability, and durability. In our investigation, we analyze the relationship between silicon thickness and key performance metrics such as efficiency, open-circuit voltage (V_{oc}), short-circuit current (J_{sc}), and fill factor (*FF*). The J-V curve of this PIN HPSC: CdTe/CISSe/Si/CdS/ZnO with Si as intrinsic absorber layer is shown in Fig. 7 (a). The variation of the thickness of Si on the performance parameters (V_{oc}, Efficiency, J_{sc} and *FF*%) of this PIN HPSC is also displayed in Fig. 7 (b). From Fig. 7 (b), we can conclude that the highest efficiency can be found when the thickness of Si can be increased up to 200 nm. Therefore, the optimized thickness has been selected as 200 nm for Si as I-layer. The performance metrics of the structures are summarized in Table 3 and Table 4 for the better understanding of the readers and for the clarity to see the results at a glance.

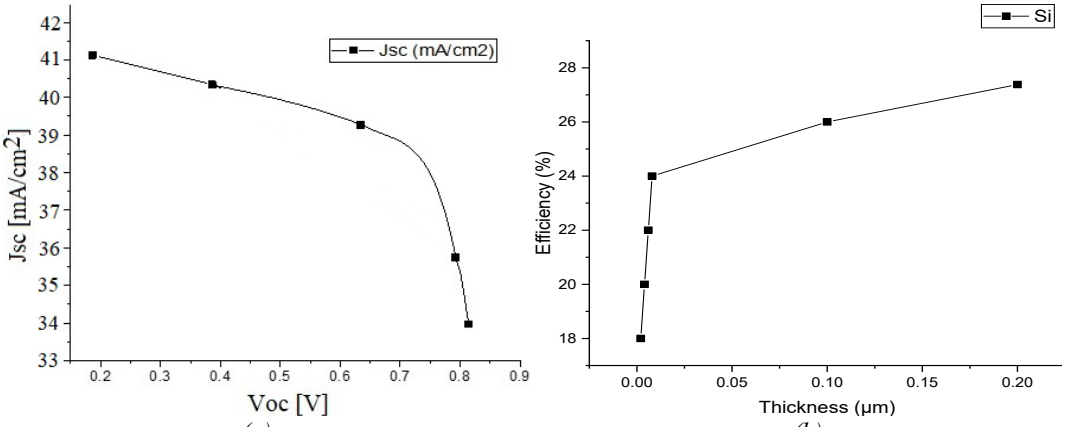

Fig. 7. (a) The J-V curve of the proposed best optimized PIN HPSC: CdTe/CISSe/Si/CdS/ZnO with Si as intrinsic Absorber layer. (b)The variation of the thickness of Si on the performance parameters (V_{oc}, efficiency, J_{sc} and FF%) of this PIN HPSC.

Table 3. Result comparison of various proposed PV structures in this work.

All attempted Structures	V_{oc} **(V)**	J_{sc} **(mA/cm^2)**	***FF*%**	**Efficiency%**
CdTe/CISSe/Si/CdS/ZnO	0.8316	41.17428	79.36%	**27.38%**
CdTe/CISSe/CdS/ZnO	0.8116	30.9868	83.52%	**21.06%**
CdTe/CISSe/CdS	0.8110	30.9836	83.35%	20.90%
CdTe/ CISSe/CdS/SnO_x	0.8079	30.9159	79.10%	19.78%
CdTe/CdS/SnO_x	0.9753	24.3360	68.64%	16.29%
CdTe/CISSe/SnO_2/TiO_2	0.8826	28.8559	77.13%	19.64%
CdTe/SnO_2/CdS	0.9373	24.9932	71.78%	16.70%

Table 4. Result comparison of the best optimized PV structures with and without Si.

Structures	V_{oc} **(V)**	J_{sc} **(mA/cm^2)**	***FF*%**	**Efficiency%**
CdTe/CISSe/Si/CdS/ZnO	0.8136	41.1436	79.36%	**27.38%**
CdTe/CISSe/CdS/ZnO	0.8116	30.9868	83.52%	**21.06%**

4. Conclusions

This paper presents a systematic examination of six different configurations of PN and high-efficiency PIN devices, which were modeled and evaluated using the SCAPS-1D simulator. Through simulations and optimization processes involving variations in layer thickness, the devices were refined to achieve optimal figures of merit. The highest power conversion efficiency (PCE) of 21.06% was attained by the best optimized PN-type solar cell, comprising p-CdTe/p-CISSe/n-CdS/n-ZnO layers. Additionally, an efficiency of 27.38% was achieved by the proposed PIN-type solar cell, involving p-CdTe/p-CISSe/Si (I)/n-CdS/n-ZnO layers, with silicon acting as a thin I-type absorber layer and CdTe serving as a suitable wide P-type exciton generation layer.

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