

Electrical characteristics and conductive mechanisms of AlN-based memristive devices

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Aluminum nitride (AlN) memristive devices have attracted a great deal of attention because of their compatibility with the CMOS fabrication technology, and more likely to be extended to power electronic devices. However, the conductive mechanism and the variability of resistance switching (RS) parameters are major issues for commercial applications. In this paper, we have obtained electrical characteristics of the Al/AlN/Pt memristors under the current compliance limits of $1\ \mu\text{A}$ and $10\ \mu\text{A}$, respectively. Furthermore, the statistics of switching parameters has been done in the Set and Reset processes. Finally, a quantum point contact model has been developed to account for conducting mechanisms and shows the evolution of the conductive filament during RS transitions.

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Keywords: Aluminum nitride memristor; conductive mechanism; quantum point contact

1. Introduction

Memristive devices are one of the most promising candidates for the future neuromorphic computing systems due to their outstanding performances such as low power consumption, high speed switching, multi-state switching, CMOS-compatible fabrication, and so on.^[1-14] Among a wide variety of resistance switching (RS) materials, nitride switching materials have better process sequences and chemical compatibility with nitride electrodes, which can be relatively easily incorporated into the CMOS process for the commercial circuits fabrication.^[15-19] Moreover, nitride memristive devices are more likely to be extended to power electronic devices such as nitride compound semiconductors.^[20, 21] Among different nitride memristive materials, AlN has attracted extensive attention of researchers due to its high resistivity ($\sim 10^{14}\ \Omega\cdot\text{cm}$), high thermal conductivity (285 W/m·K) and wide band gap (6.2 eV)^[22, 23]. It has been reported that these properties will help the memristor to suppress the thermal effect of the dielectric layer, thereby enhancing the controllability of the conductive filament and reducing the operating current.^[24] In addition, AlN has its good CMOS process compatibility, thermal stability and chemical stability, which will help to avoid the formation of unstable interfaces and reduce the fabrication cost during the fabrication of AlN memristors.^[25] According to recent reports AlN-based memristors exhibit

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ultrafast ON/OFF switching times(85 ps) at low operating currents(15 μ A).^[26] In the research of neuromorphic computing, artificial electronic synapses composed of wide band gap III-V materials represented by AlN have been confirmed to have wider dynamic range and better linearity.^[27]

Recently, it has been found that AlN memristors exhibit volatile threshold switching characteristics in addition to non-volatile switching characteristics.^[25, 28]; this discovery will help broaden the scope of application fields of AlN memristors. The spiking neural network (SNN) has most recently become a hot research topic due to its closer approximation to the real biological neuron system and lower data computing power consumption. Threshold-switching memristors with volatile properties excitingly exhibited a capability of constructing integrate-and-fire (LIF) neurons for SNNs,^[29, 30] thus paving a path for AlN based memristor towards the neuro-synapse mimics. Note that the magnitude of the operating current has been found to affect the volatile nature of AlN memristors,^[28] thus becoming one of the important factors of the volatile characteristics of AlN memristors.

In spite of its promising prospect, a comprehensive study on volatile mechanisms and the variability of switching parameters of the AlN memristors is still missing, thus preventing the advancement of aluminum nitride memristive devices from research labs to industry applications.^[31-34] In order to address these issues, we here have fabricated aluminum nitride (AlN) memristive devices and successfully got their electrical characteristics. First of all, we analyzed the electrical characteristics and did the statistics of RS parameters for both the ON and OFF states. Then a quantum point contact (QPC) model was applied to identify the conductive mechanisms and observe the transition into a conductive filament (CF) during the switching processes.

2. Device fabrications

The studied Al/AlN/Pt memristive devices consisted of a 6 nm RS layer AlN thin film deposited by atomic layer deposition (ALD) using Trimethylaluminum (TMA, Al (CH₃)₃) and N₂:H₂ (20:40 SCCM) mixed gas as a metal organic precursor and a reactant gas at a water temperature of 350 °C. Metallic Al and Pt layers were deposited by electron-beam evaporation (EBV) at ambient temperature. The sandwich structure of the Al/AlN/Pt devices consisted of (from bottom to top) a 20 nm Pt bottom electrode (BE), a 6 nm aluminum nitride switching layer, and a 15 nm Al top electrode (TE). Additionally, a 25 nm Pt film was deposited over the Al without breaking the vacuum to minimize Al oxidation. Such devices were located at the cross points of Pt top electrode rows and Pt bottom electrode columns, as illustrated in Figure 1, to be compatible with future integrated circuit design, which has been widely adopted by previous work.^[35]

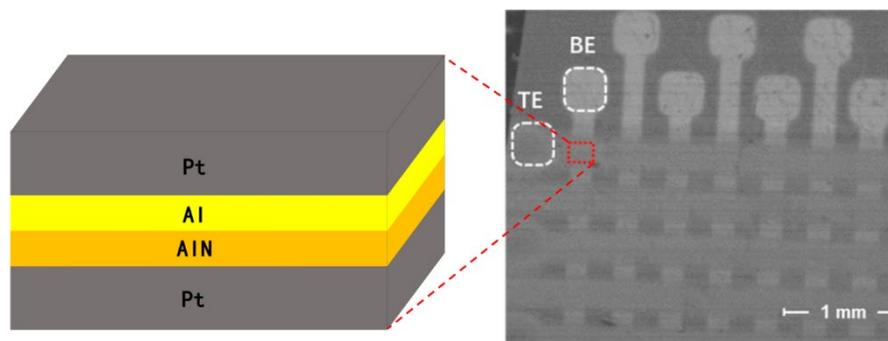


Fig. 1. The designed memristive stack (left) and the scanning electron microscopy image (right) of the crossbar array where the designed memristive stacks are integrated. Reprinted permission from [35].

For such crossbar design, the perpendicular and horizontal bars of the array correspond to the bottom and top Pt electrodes, respectively, while each memristive device is bounded by the red dash. The pad size, confined by the white dash, is $300\ \mu\text{m}$ by $300\ \mu\text{m}$. The Current–Voltage (I – V) switching curves and conductance measurements were performed by using an Agilent B1500 semiconductor parameter analyzer, while resistance measurement was performed by Keithley 4200 parameter analyzer to provide different compliance current under pulse module. After the electroforming operation, long lasting repetitive cycling experiments were performed using voltage ramp stress both for Set and Reset processes.

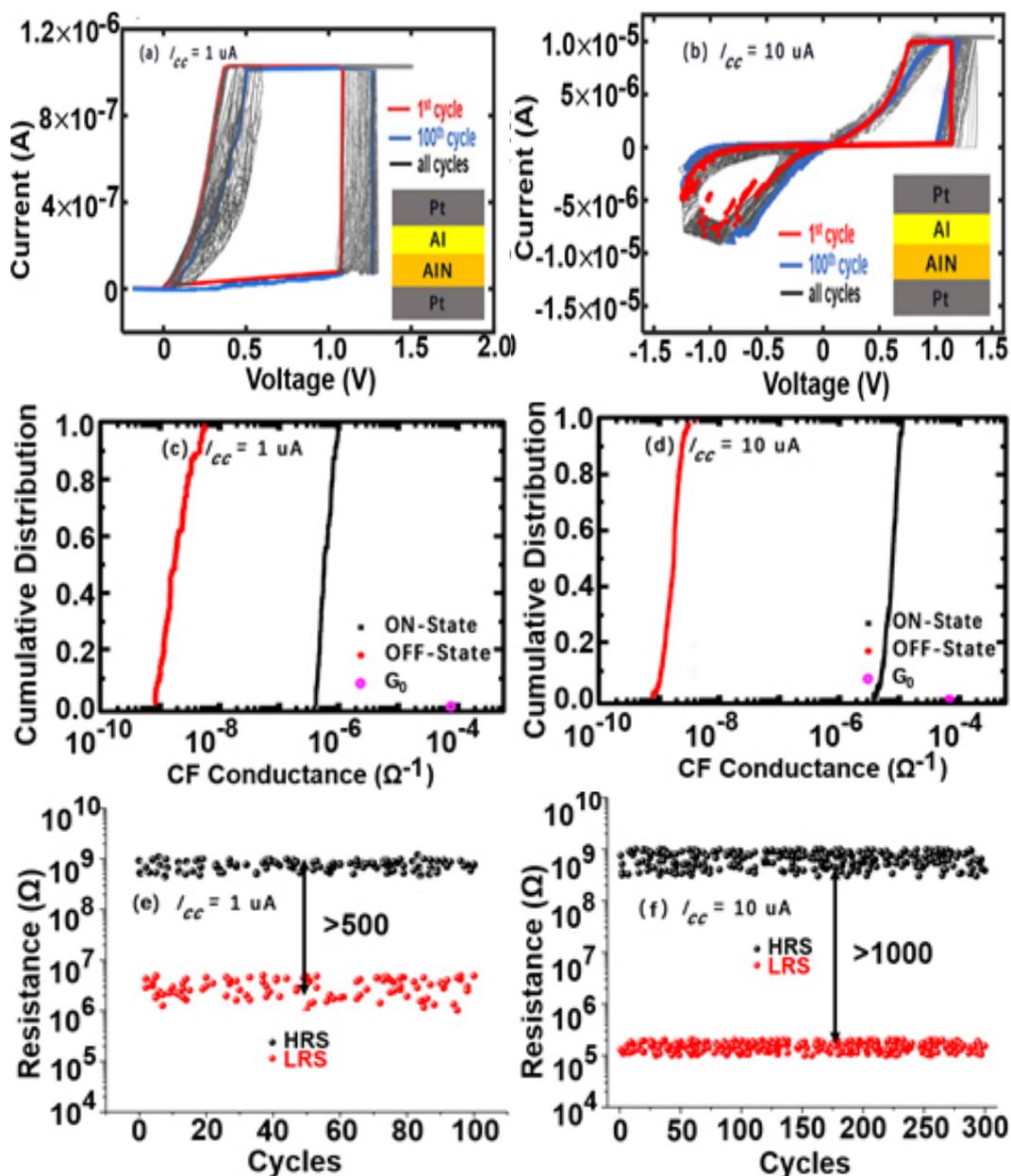


Fig. 2. The typical I – V characteristics curves of the Set and Reset processes in the Al/AIN/Pt memristor under the current compliance limits of (a) $1\ \mu\text{A}$ and (b) $10\ \mu\text{A}$, respectively. The cumulative distribution of CF conductance in both ON and OFF states for 100 cycles under the current compliance limits of (c) $1\ \mu\text{A}$ and 300 cycles under the current compliance limits of (d) $10\ \mu\text{A}$, respectively. Endurance performances of the studied device for 100 cycles under the current compliance limits of (e) $1\ \mu\text{A}$ and 300 cycles under the current compliance limits of (f) $10\ \mu\text{A}$, respectively, obtained from 20 ms pulses.

3. Results and discussions

To investigate the low-power consumption Al/AlN/Pt memristors, relatively low current compliance limits (I_{CC}) of $1\ \mu\text{A}$ and $10\ \mu\text{A}$ were given in the Set processes. Figs. 2(a) and 2(b) show the typical I - V switching curves under the current compliance limits of $1\ \mu\text{A}$ and $10\ \mu\text{A}$ for 100 cycles, respectively. For both cases, resulting I - V curves exhibit good consistency among different cycles. In terms of Fig. 2(a), the device initially remains in a high-resistance state (HRS) when the applied bias is below approximately 1.25 V. Once the applied bias exceeds 1.25 V, device resistance is reduced abruptly, thus exhibiting a low-resistance state (LRS). This implies a SET voltage of 1.25 V. It is also found that such LRS can be maintained as long as the applied bias is greater than 0.25 V. When further reducing the bias below 0.25 V, device resistance is switched back to its HRS. Such HRS can be sustained even if the device is subjected to a negative bias, consequently giving rise to a volatile switching characteristic, also known as threshold switching. For Fig. 2(b) with high compliance current, a bipolar switching behavior, known as resistive switching, occurs in the Al/AlN/Pt memristors, i.e., Set to the LRS under positive voltages and Reset to the HRS under negative voltages. Moreover, it can be observed that the I - V switching curves under $I_{CC} = 10\ \mu\text{A}$ are more symmetric in two different polarities than $I_{CC} = 1\ \mu\text{A}$. Moreover, cycling measurements were performed on the Al/AlN/Pt memristive device for 100 cycles under $I_{CC} = 1\ \mu\text{A}$ and 300 cycles under $I_{CC} = 10\ \mu\text{A}$. Then, we extracted different CF conductance in both the ON and OFF states, calculated at 0.1 V. Figs. 2(c) and 2(d) present the cumulative distributions of the ON and OFF conductance under $I_{CC} = 1\ \mu\text{A}$ and $I_{CC} = 10\ \mu\text{A}$, respectively. It is worth noting that the CF conductance in both the ON and OFF states are less than quantum conductance $G_0 = 2e^2/h$ (where e and h are the electron charge and the Planck constant) under the current compliance limits of $1\ \mu\text{A}$ and $10\ \mu\text{A}$, which means just one single CF is formed in Al/AlN/Pt memristive device due to $G < G_0$. Next, we would focus on RS parameters and conductive mechanisms of Al/AlN/Pt memristive devices under $I_{CC} = 10\ \mu\text{A}$, the same methods and conclusions applied to $I_{CC} = 1\ \mu\text{A}$. Pulse endurance tests were also performed for different current compliance limits using 20 ms pulses, as illustrated in Figs. 2(e) and 2(f). It is clearly observed that for both current compliance limits, its HRS can be distinguished from the LRS, demonstrating its readability. The On-Off ratios are found to be approximately 500 and 1000 for I_{CC} of $1\ \mu\text{A}$ and $10\ \mu\text{A}$, respectively. Such high On-Off ratio can be remained after 300 cycles, particularly for the case of $10\ \mu\text{A}$ I_{CC} . However, relatively strong resistance fluctuation is also noticed among different cycles for both case, which can be mainly ascribed to the stochastic nature of the nucleation and growth of the CF.

The statistics of RS parameters versus the initial CF conductance has been determined in both the ON and OFF states for $I_{CC} = 10\ \mu\text{A}$, and are shown in Fig. 3. Figs. 3(a) and 3(b) show the Reset voltage and Reset current (V_{Reset} and I_{Reset}) versus the initial ON-state conductance (G_{ON}), extracted at 0.1 V. It can be seen that V_{Reset} is nearly independent of G_{ON} , whereas I_{Reset} is proportional to G_{ON} . This observation result is consistent with the thermal-activated dissolution model.^[36, 37] In this model, the Reset event occurs only when the temperature of the CF reaches a critical value. Figs. 3(c) and 3(d) show the Set voltage and Set current (V_{Set} and I_{Set}) versus the initial OFF-state conductance (G_{OFF}), also calculated at 0.1 V. It can be seen that V_{Set} is inversely proportional to G_{OFF} whereas I_{Set} is proportional to G_{OFF} . According to the statistics of RS parameters, we can acquire that the distributions of switching parameters are strongly influenced by the initial CF conductance. Therefore, we can improve the performances of Al/AlN/Pt memristors by adjusting the distributions of G_{ON} and G_{OFF} before the ON and OFF switching.

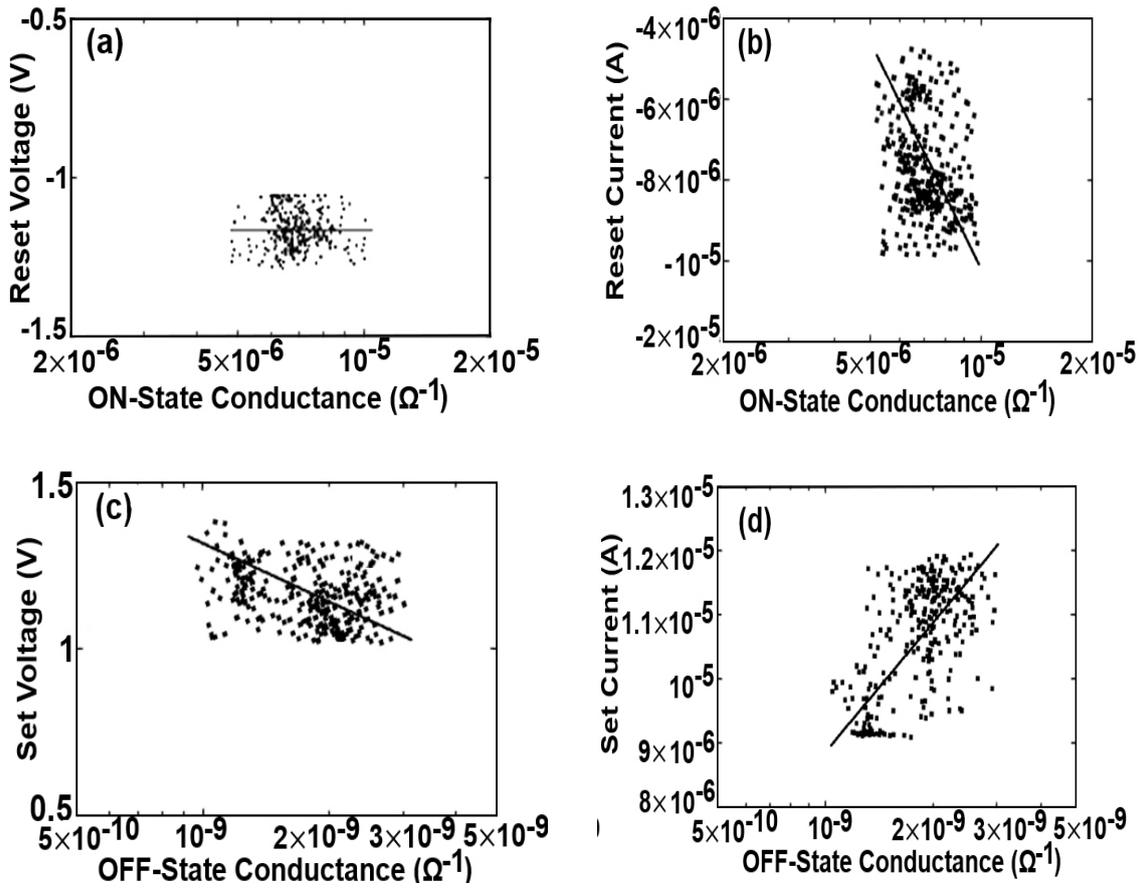


Fig. 3. The statistics of RS parameters in Al/AlN/Pt memristor under the current compliance limits of $10 \mu\text{A}$. (a) Reset voltage and (b) Reset current versus the initial ON-State conductance for 300 cycles experimental data in the same device. (c) Set voltage and (d) Set current versus the initial OFF-State conductance for 300 cycling experimental data in the same device.

In view of the above observations, a quantum point contact (QPC) model is suitable to study the conductive mechanisms and the CF transformation between the ON and OFF states. The QPC model is based on the Landauer transmission approach to calculate conduction along narrow microscopic constrictions. [38, 39] According to the Landauer's approach, the current flowing through a CF with N vacancy paths can be computed as: [40]

$$I(V) = \frac{2e}{h} N \int_{-\infty}^{\infty} T(E) \{ f(E - \beta eV) - f(E + (1 - \beta)eV) \} dE \quad (1)$$

where E is the energy, $T(E)$ is the transmission probability, f is the Fermi-Dirac distribution function, β is the averaged asymmetry parameter ($0 < \beta \leq 1$), and V is the applied voltage assumed to drop at the cathode and anode interfaces with a fraction of β and $(1 - \beta)$, respectively, shown in Fig. 4.

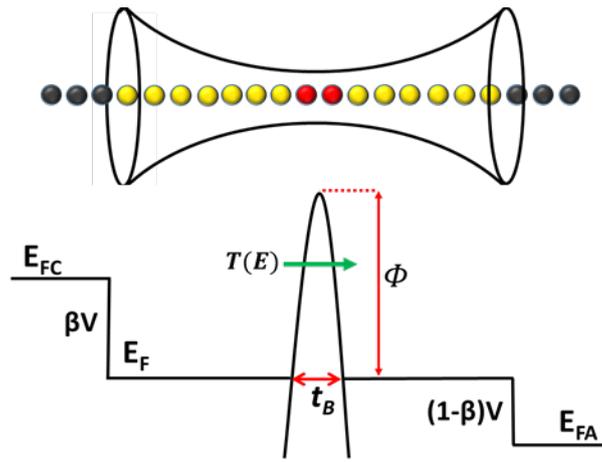


Fig. 4. The QPC model used into the Al/AlN/Pt memristors. Two re-oxidized vacancies of one single CF path would develop a barrier for electron transport. The applied voltage of V which is assumed to drop at the cathode and anode interfaces with a fraction of β and $(1-\beta)$, respectively.

The CF conductance can be calculated by using a Green's function formalism combined with a density functional theory code.^[41-44] It shows that one vacancy path could form a conductive channel, with a conductance of the order of G_0 .^[45, 46] Each time a vacancy is removed from one single vacancy path, the barrier would be introduced and the conductance of CF decreases by a factor of ~ 10 , which has been revealed in hafnium oxide memristors.^[47, 48] Taking into consideration of an inverted parabolic potential barrier, we can obtain an expression for the tunneling probability,^[49-51] $T(E) = \{1 + \exp[-\alpha(E - \Phi)]\}^{-1}$, where Φ is the barrier height and $\alpha = t_B \pi^2 \hbar^{-1} \sqrt{2m^*/\Phi}$ is related to the inverse of potential barrier curvature, m^* is the effective electron mass and t_B is the barrier width at the equilibrium Fermi energy, assumed to be equal to t_{gap} . Inserting the tunneling probability into equation (1), we can obtain:

$$I = \frac{2e}{h} N \left\{ eV + \frac{1}{\alpha} \text{Ln} \left[\frac{1 + \exp\{\alpha[\Phi - \beta eV]\}}{1 + \exp\{\alpha[\Phi + (1-\beta)eV]\}} \right] \right\} \quad (2)$$

Because $G < G_0$ in both the ON and OFF states, we can assume that there is one single CF vacancy path ($N = 1$) connecting the TE and BE for the Al/AlN/Pt memristor. To simplify the I - V fitting process, here we set $N = 1$, and $\beta = 1$ by taking into account of the asymmetry device structure. Then, we collected the barrier height Φ and the average barrier thickness t_B according to fit 300 cycles experimental data by using the least-square-estimation (LSE) method and equation (2). The I - V fitting results are good in both log scale and linear scale, shown in Figs. 5(a) and 5(b). Furthermore, Figs. 5(c) and 5(d) show the exacted QPC parameters versus the initial CF conductance. The perfect straight line in Fig. 5(c) indicates that the CF conductance is fully determined by the product of $\alpha\Phi$ in both the ON and OFF states. The extrapolation of this straight line to $\alpha\Phi = 0$ (the transmission probability equal to 1) converges to a CF conductance equal to G_0 (purple circle), which show that the QPC model is consistent and in good agreement with the experimental CF conduction properties. From the above formula $\alpha = t_B \pi^2 \hbar^{-1} \sqrt{2m^*/\Phi}$, we know that the value of t_B is determined by the values of α and Φ . Therefore, the initial CF conductance is also determined by t_B , shown in Fig. 5(d). The conductance of CF is G_0 when a complete quantum wire (no barrier) is formed in the Al/AlN/Pt memristors. When a vacancy is removed from a single vacancy path, the barrier would be produced and the conductance is reduced by a factor of ~ 10 . The average t_{gap} is approximately 0.5 nm in the ON-state, which is about two re-oxidized vacancy gap opened in the CF, and the average t_{gap} in the OFF-state is about 0.75 nm, which are about three re-oxidized vacancy gap formed in the CF. Thus, after

electroforming operation, one single CF vacancy path would form in the Al/AlN/Pt memristors along with the gap changing between the ON and OFF states.

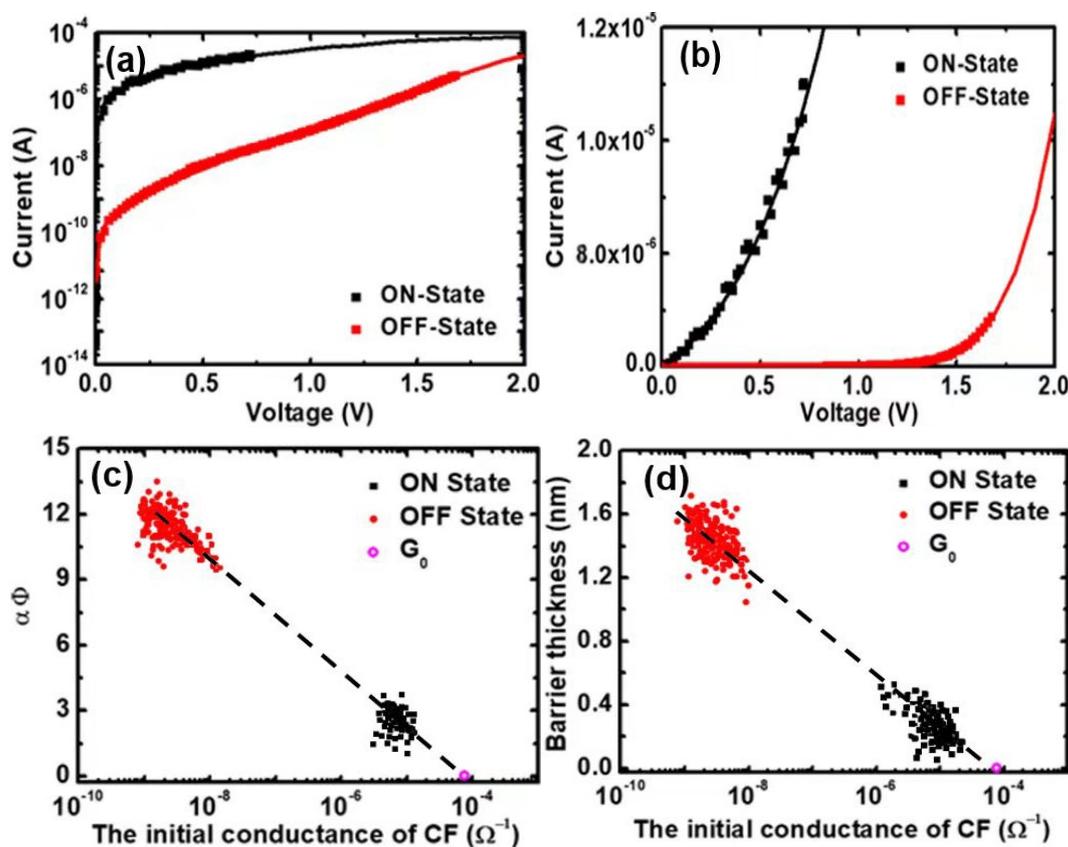


Fig. 5. The experimental data (scatter points) and fitting results of QPC model (solid line) for both the ON and OFF states (a) in log and (b) linear scales. (c) The product $\alpha\Phi$ and (d) the barrier thickness versus the initial conductance of CF respectively. The averaged values are: $\langle t_{gap} \rangle = 0.5$ nm in the ON-State and $\langle t_{gap} \rangle = 0.75$ nm in the OFF-State.

Combining the simulation results of QPC model with experimental RS characteristics, the conductive mechanisms of switching processes can be proposed for the Al/AlN/Pt memristors. The CF may consist of nitrogen vacancies and formed by a quantum point contact within the AlN layer and broken by thermally activated atomic-scale fluctuations. The Al top electrode is believed to act as a nitrogen extraction layer and to introduce a quantity of nitrogen vacancies in the AlN layer. After the electroforming operation, one single CF vacancy path would form in the Al/AlN/Pt memristive devices. In the LRS, about two re-oxidized vacancy gap opened in the CF, then the gap increases to three vacancies in the HRS. The active region of the CF during RS is deduced to be near the bottom electrode due to asymmetric device structure. It should be kept in mind that changing the AlN layer thickness may impact the device switching characteristics, particularly the SET voltages. This is because a critical electric field is usually required to facilitate the vacancies migration to form a CF that connects top electrode and bottom electrode.^[52] Under this circumstance, a thicker AlN layer can naturally result in higher SET voltage. Similar to the SET process, a thicker AlN layer also requires larger RESET voltage to generate sufficient Joule heating to break the CF. Based on above analysis, increasing the AlN layer can cause higher SET and RESET voltages. However, this might not be the case for very thick layer. When further thickening the AlN layer thickness, incomplete rupture of the CF is likely to be achieved.^[53] In this case, the SET process only needs to restore this local region other than the entire CF. For above reasons, further thickening the AlN thickness may not be sensitive to its SET and RESET voltages.

It is obvious that the stochastic nature of the formation and rupture of the CFs causes their location difficult being established, severely deteriorating the physical performances of the proposed device. The main driving force behind the CF formation and rupture can be attributed to the electric field. However, using planar top and bottom electrodes usually results in a uniform distribution of the electric field across the whole AlN layer, thus causing stochastic nucleation and growth of the CF. In this case, it might be possible to use a cone shaped top electrode to replace the conventional planar top electrode.^[54] Due to its sharp edge, the cone-shaped top electrode enables highly concentrated electric field at cone tip. Owing to its strong intensity, resulting CF can be directly formed underneath the cone and grow towards the bottom electrode. This makes the CF easily be controlled, thus suppressing its stochastic nature. Such strategy can be also applied to the bottom electrode by replacing conventional planar bottom electrode with nanocrystal covered bottom electrode.^[55] Table 1 shows the performances comparison between the device presented here and previously reported devices. It is found that the device architecture presented here, based on the vacancies conduction mechanism, differs from previously reported devices that adopted active top electrodes, governed by the metal ions conduction mechanism. Additionally, our work exhibits lower SET voltage and larger cycles than those using active top electrodes, demonstrating its low energy consumption and better reliability.

Table 1. Performance comparison between our work and previously reported work.

Device structure	$V_{Set}(V)$	$V_{Reset}(V)$	I_{CC}	Cycles	Mechanism
Cu/AlN/TiN ^[28]	2.602	-1.033	10 μ A	100	Metal ions CF
TiN/AlN/Pt ^[12]	0.65	-0.65	1mA	100	Nitrogen vacancies CF
Pt/AlN/Cu/AlN/Pt ^[25]	2.4	-1.7	NA	50	Metal ions CF
Our work	1.25	-1.25	10 μ A	300	Nitrogen vacancies CF

4. Conclusions

In conclusion, the electrical characteristics and conductive mechanisms have been studied in AlN-based memristive devices. Through the statistics of RS parameters, we know that the distributions of switching parameters are strongly influenced by the initial CF conductance. The performances of Al/AlN/Pt memristors can be optimized by adjusting the distributions of G_{ON} and G_{OFF} before the ON and OFF switching. In addition, the QPC model has been developed to explain the conductive mechanism and shows the evolution of the CF during RS transitions. After the electroforming operation, one single CF vacancy path would form in the Al/AlN/Pt memristors due to $G < G_0$, and vacancy gap increases from the LRS to HRS.

Acknowledgments

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